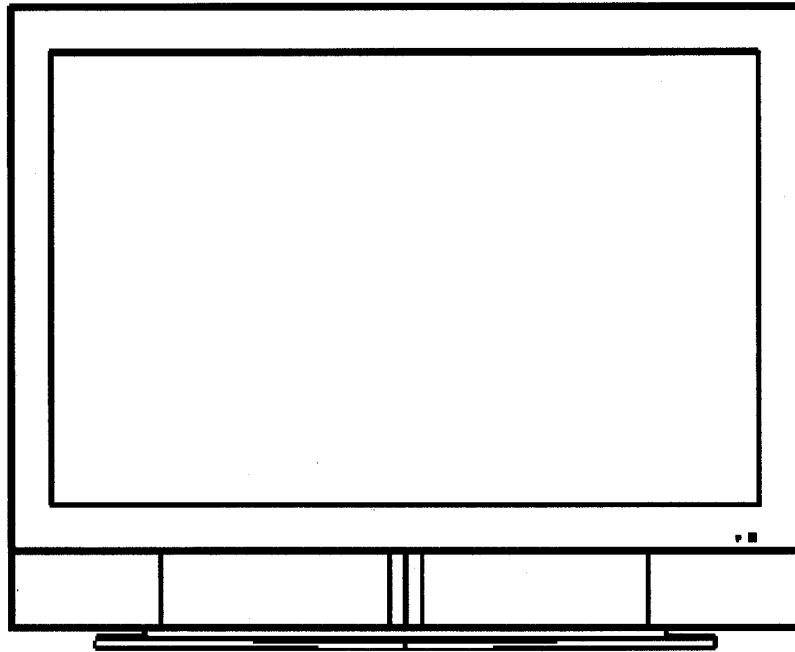
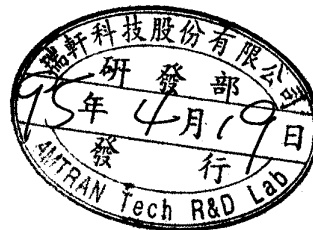


# Service Manual



**Model #: VIZIO P42HDTV10A**

V, Inc  
320A Kalmus Drive Costa Mesa, CA 92626  
TEL : +714-668-0588 FAX :+714-668-9099



*Top Confidential*

## Table of Contents

CONTENTS	PAGE
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### *Sections*

<b>1. Features</b>	<b>1-1</b>
<b>2. Specifications</b>	<b>2-1</b>
<b>3. On Screen Display</b>	<b>3-1</b>
<b>4. Factory Preset Timings</b>	<b>4-1</b>
<b>5. Pin Assignment</b>	<b>5-1</b>
<b>6. BLOCK DIAGRAM</b>	<b>6-1</b>
<b>7. Main Board I/O Connections</b>	<b>7-1</b>
<b>8. Theory of Circuit Operation</b>	<b>8-1</b>
<b>9. Waveforms</b>	<b>9-1</b>
<b>10. Trouble Shooting</b>	<b>10-1</b>
<b>11. Spare Parts List</b>	<b>11-1</b>
<b>12. Complete Parts List</b>	<b>12-1</b>

### *Appendix*

1. Main Board Circuit Diagram
2. Main Board PCB Layout
3. Assembly Explosion Drawing

Block Diagram

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#### FCC INFORMATION

This equipment has been tested and found to comply with the limits of a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that the interference will not occur in a particular installation. If this equipment does cause unacceptable interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures -- reorient or relocate the receiving antenna; increase the separation between equipment and receiver; or connect the into an outlet on a circuit different from that to which the receiver is connected.

#### FCC WARNING

To assure continued FCC compliance, the user must use a grounded power supply cord and the provided shielded video interface cable with bonded ferrite cores. Also, any unauthorized changes or modifications to Amtrak products will void the user's authority to operate this device. Thus VINC. Will not be held responsible for the product and its safety.

#### CE CERTIFICATION

This device complies with the requirements of the EEC directive 89/336/EEC with regard to "Electromagnetic compatibility."

#### SAFETY CAUTION

Use a power cable that is properly grounded. Always use the AC cords as follows – USA (UL); Canada (CSA); Germany (VDE); Switzerland (SEV); Britain (BASEC/BS); Japan (Electric Appliance Control Act); or an AC cord that meets the local safety standards.

# Chapter 1      Features

---

- 1024 x 768 pixel resolution with 16:9 wide screen
- ATSC (Off-air)/QAM (Cable)/NTSC (Antenna/Cable)
- All TV formats supported (480i, 480p, 720p & 1080i)
- PC compatible (RGB) up to 1280 x 1024 WXGA
- High definition digital interface - HDMI
- Multiple-screen display (picture-on-picture/picture-in-picture)
- Selectable picture mode
- Supporting DVI converted to HDMI
- Closed caption
- Gloss front bezel
- Wall-mountable

# Chapter 2 Specification

---

## 1. General specification

<i>Native Resolution</i>	1024 (H)X768 (V) pixels,
<i>Effective Display Size</i>	921.6 (H) x 519.2 (V) mm
<i>Aspect Ratio</i>	16:9
<i>Color</i>	1,024 (R) x 1,024 (G) x 1,024 (B) colors
<i>Brightness</i>	1200 cd/m <sup>2</sup> ( typical, panel spec)
	(w/glass filter) Min. 300 cd/ m <sup>2</sup>
<i>Contrast Ratio</i>	10,000:1 (Typical, panel spec).
<i>TV system</i>	NTSC/ATSC/ QAM
<i>PC Inputs</i>	15pins D-sub, HDMI-DVI
<i>Video Inputs</i>	1 x S-Video
	3 x AV inputs (CVBS; RCA type)
	2 x Component (Y Pb/Pr Cb/Cr)
	1 x HDMI
<i>Audio Inputs</i>	6 x Stereo RCA (R/L), 1 x PC Mini-Jack
<i>Audio Outputs</i>	Analog - 1 x stereo RCA (R/L)
	1 x headphone
	Digital – 1 x SPDIF Optical
<i>Audio</i>	10W 6Ω X 2
<i>Power Input</i>	100 to 240 Vac
<i>Power Consumption</i>	380W Max
<i>Preset Modes</i>	Primary 1024 x 768 @ 60Hz.

---

## 2. Optical characteristics

Item	Specification	Remarks
Display Pixels	1,024 (H) x 768 (V) pixels	
Display Cells	3,072 (H) x 768 (V) cells	
Pixel Pitch	0.9 (H) x 0.676 (V) mm	
Pixel Type	Non-stripe	
Color Depth	1,024 (R) x 1,024 (G) x 1,024 (B) colors	
Active Display Area	921.6 (H) x 519.2 (V) $\pm 0.5$ mm	
Brightness	Min. 300 cd/ m <sup>2</sup>	
Color coordinates	9300K: x=0.283 $\pm$ 0.02, y=0.297 $\pm$ 0.02	RGB
	6500K: x=0.313 $\pm$ 0.02, y=0.329 $\pm$ 0.02	RGB /VIDEO
	5000K: x=0.346 $\pm$ 0.02, y=0.359 $\pm$ 0.02	RGB

## 3. Power Supply

- a. Input voltage 100-240Vac, 50/60Hz
- b. Input current 4.5A or less (at AC 100V/60Hz)
- c. Inrush current 60A at Vac=120V
- d. Power consumption 380 W Max
- e. Standby/DPMS 3 watts max. (at 120 Vac)

## 4. Environment

### Operating

- a. Temperature: 0~40°C
- b. Relative humidity: 20%~80% RH
- c. Altitude: 0~6,560 ft

### Non-operating

- a. Temperature: -20~60°C
- b. Relative humidity: 10%~90% RH
- c. Altitude: 0~9,840 ft

---

## 5. Dimensions

Item	W/Stand	W/O stand
a. Height	780 mm	755 mm
b. Width	1072mm	1072mm
c. Depth	290 mm	109 mm

## 6. Weight

- a. Net: 38.8 +/- 0.5 kgs
- b. Gross: 47.5 +1.5 kgs /- 0.5 kgs

## Chapter 3 On Screen Display

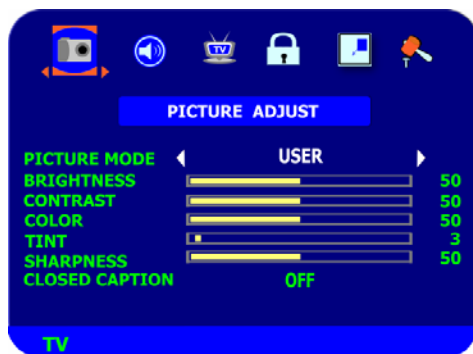
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### Input Menu



### Operation Menu

#### TV Mode



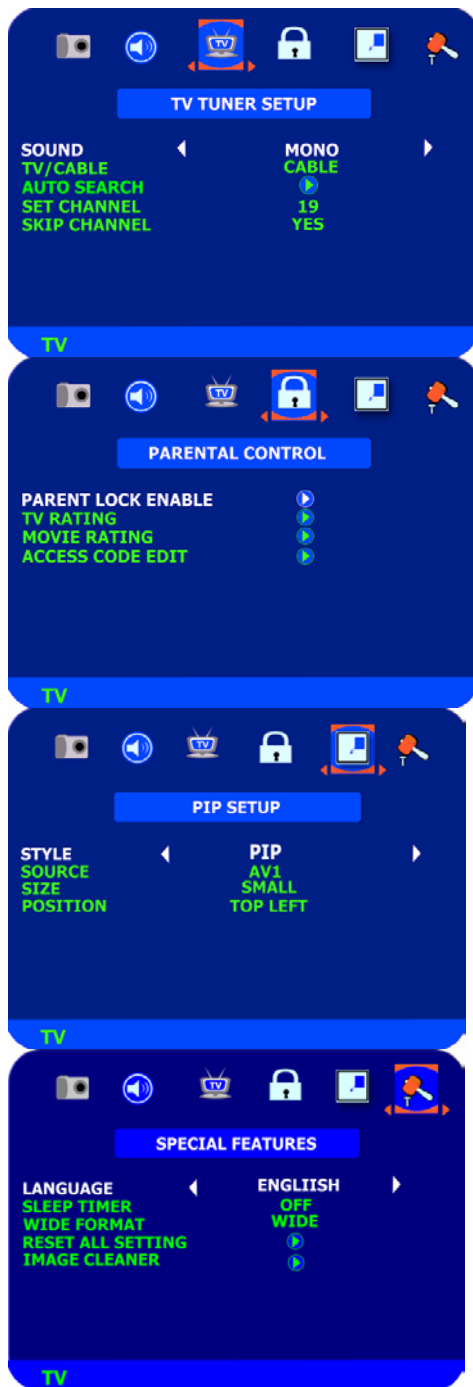
#### A. PICTURE ADJUST :

- PICTURE MODE (USER/ VIVID1 / VIVID2 / VIVID3)
- Adjust the BRIGHTNESS (0~100)
- Adjust the CONTRAST (0~100)
- Adjust the COLOR (saturation) (0~100)
- Adjust the TINT (hue) (0~100)
- Adjust the SHARPNESS (0~100)
- CLOSED CAPTION  
(OFF/CC1/CC2/CC3/CC4/TT1/TT2/TT3/TT4)



#### B. AUDIO ADJUST :

- VOLUME (0~100)
- BASS (-50~50)
- TREBLE (-50~50)
- BALANCE (-50~50)
- SURROUND (ON/OFF)
- REVERB (OFF, CONCERT, LIVING ROOM, HALL, ARENA)
- MUTE (ON/OFF)
- SPEAKERS (ON/OFF)



#### C. TV TUNER SETUP :

- SOUND (SAP/MONO/STEREO)
- TV/CABLE (TV/CABLE)
- CHANNEL SEARCH (RUN)
- SET CHANNEL
- SKIP CHANNEL (YES/NO)

#### D. PARENTAL CONTROL :

- PARENT LOCK ENABLE (ON/OFF)
- TV RATING
- MOVIE RATING
- ACCESS CODE EDIT

#### E. PIP SETUP :

- STYLE (OFF/PIP/POP)
- Source (AV1 、 AV2 、 AV3 、 ANALOG HD1 、 ANALOG HD2 、 DIGITAL HD 、 RGB)
- SIZE (SMALL/MEDIUM/LARGE)
- POSITION (TOP LEFT/TOP CENTER/TOP RIGHT/MIDDLE LEFT/MIDDLE RIGHT/BOTTOM LEFT/BOTTOM CENTER/BOTTOM RIGHT)

#### F. SPECIAL FEATURES :

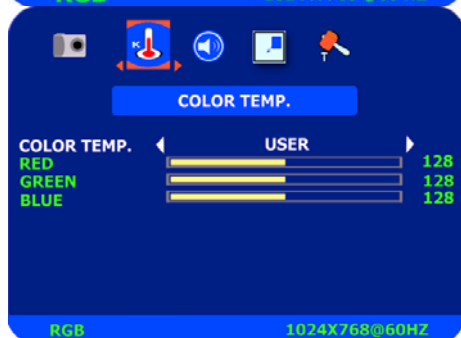
- LANGUAGE (ENGLISH/FRANÇAIS/ ESPAÑOL)
- SLEEP TIMER (OFF/30 MIN /60 MIN /90 MIN /120 MIN)
- WIDE FORMAT (NORMAL/WIDE/ZOOM 、 PANORAMIC)
- RESET ALL SETTING
- IMAGE CLEANER

## RGB Mode



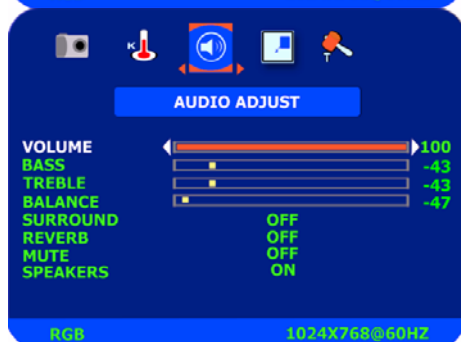
### A. PICTURE ADJUST :

- AUTO ADJUST
- Adjust the BRIGHTNESS (0~100)
- Adjust the CONTRAST (0~100)
- Adjust the H-SIZE (0~100)
- Adjust the H-POSITION (0~100)
- Adjust the V-POSITION (0~100)
- Adjust the FINETUNE (0~100)



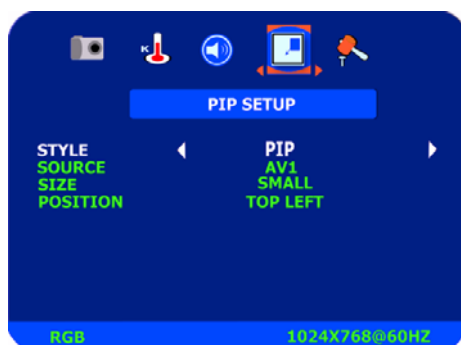
### B. COLOR TEMP :

- COLOR TEMP. (User, 5000K, 6500K, 9300K)
- RED (0~255)
- GREEN (0~255)
- BLUE (0~255)



### C. AUDIO ADJUST :

- VOLUME (0~100)
- BASS (-50~50)
- TREBLE (-50~50)
- BALANCE (-50~50)
- SURROUND (ON/OFF)
- REVERB (OFF, CONCERT, LIVING ROOM, HALL, ARENA)
- MUTE (ON/OFF)
- SPEAKERS (ON/OFF)



### D. PIP SETUP :

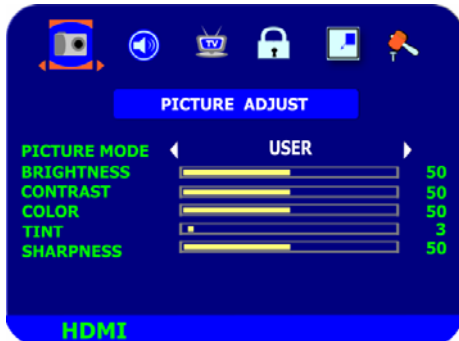
- STYLE (OFF/PIP/POP)
- SOURCE (AV1, AV2, AV3, TV)
- SIZE (SMALL/MEDIUM/LARGE)
- POSITION (TOP LEFT/TOP CENTER/TOP RIGHT/MIDDLE LEFT/MIDDLE RIGHT/BOTTOM LEFT/BOTTOM CENTER/BOTTOM RIGHT)



#### E. SPECIAL FEATURES :

- LANGUAGE (ENGLISH/FRANÇAIS/ESPAÑOL)
- SLEEP TIMER (OFF/30/60/90/120)
- WIDE FORMAT (WIDE/NORMAL)
- RESET ALL SETTING
- IMAGE CLEANER

## HDMI Mode



#### A. PICTURE ADJUST :

- PICTURE MODE (USER/ VIVID1 / VIVID2 / VIVID3)
- Adjust the BRIGHTNESS (0~100)
- Adjust the CONTRAST (0~100)
- Adjust the COLOR (saturation) (0~100)
- Adjust the TINT (hue) (0~100)
- Adjust the SHARPNESS (0~100)



#### B. AUDIO ADJUST :

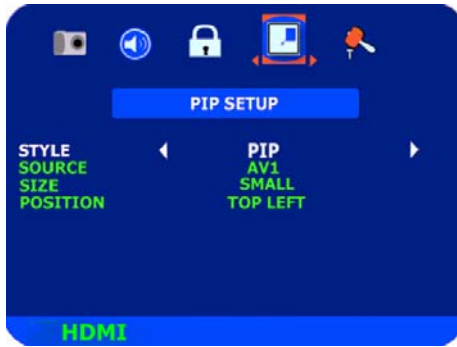
- VOLUME (0~100)
- BASS (-50~50)
- TREBLE (-50~50)
- BALANCE (-50~50)
- SURROUND (ON/OFF)
- REVERB (OFF, CONCERT, LIVING ROOM, HALL, ARENA)
- MUTE (ON/OFF)
- SPEAKERS (ON/OFF)
- AUDIO SOURCE (HDMI/DVII)

NOTE: While main or pip exists HDMI source, audio option will add an AUDIO SOURCE item.

#### C. PARENTAL CONTROL :

- PARENT LOCK ENABLE (ON/OFF)
- TV RATING
- MOVIE RATING
- ACCESS CODE EDIT





#### D. PIP SETUP :

- STYLE (OFF/PIP/POP)
- SOURCE (AV1 、 AV2 、 AV3 、 TV)
- SIZE (SMALL /MEDIUM/LARGE)
- POSITION (TOP LEFT/TOP CENTER/TOP RIGHT/MIDDLE LEFT/MIDDLE RIGHT/BOTTOM LEFT/BOTTOM CENTER/BOTTOM RIGHT)



#### E. SPECIAL FEATURES :

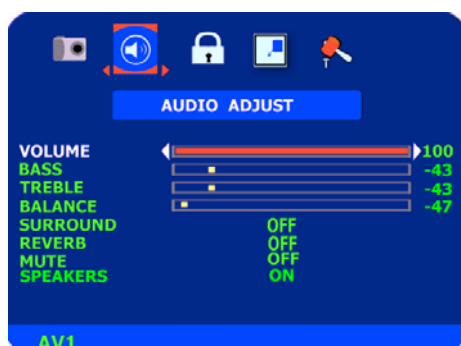
- LANGUAGE (ENGLISH/FRANÇAIS/ ESPAÑOL)
- SLEEP TIMER (OFF/30/60/90/120)
- WIDE FORMAT (NORMAL/WIDE/ZOOM)
- RESET ALL SETTING
- IMAGE CLEANER

## Video Mode -AV1、AV2、AV3、COMPONENT 1、COMPONENT 2



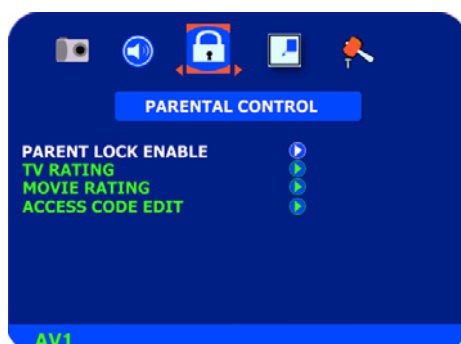
### A. PICTURE ADJUST :

- PICTURE MODE (USER/ VIVID1 / VIVID2 / VIVID3)
- Adjust the BRIGHTNESS (0~100)
- Adjust the CONTRAST (0~100)
- Adjust the COLOR (saturation) (0~100)
- Adjust the TINT (hue) (0~100)
- Adjust the SHARPNESS (0~100)
- CLOSED CAPTION  
(OFF/CC1/CC2/CC3/CC4/TT1/TT2/TT3/TT4)



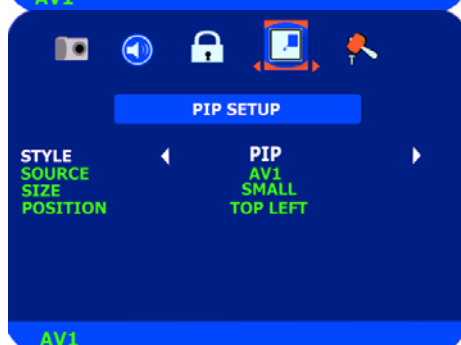
### B. AUDIO ADJUST :

- VOLUME (0~100)
- BASS (-50~50)
- TREBLE (-50~50)
- BALANCE (-50~50)
- SURROUND (ON/OFF)
- REVERB (OFF, CONCERT, LIVING ROOM, HALL, ARENA)
- MUTE (ON/OFF)
- SPEAKERS (ON/OFF)



### C. PARENTAL CONTROL :

- PARENT LOCK ENABLE (ON/OFF)
- TV RATING
- MOVIE RATING
- ACCESS CODE EDIT



### D. PIP SETUP :

- STYLE (OFF/PIP/POP)
- SOURCE (AV2, AV3, COMPONENT 1, COMPONENT 2, HDMI, RGB, TV, DTV)
- SIZE (SMALL/MEDIUM/LARGE)
- POSITION (TOP LEFT/TOP CENTER/TOP RIGHT/MIDDLE LEFT/MIDDLE RIGHT/BOTTOM LEFT/BOTTOM CENTER/BOTTOM RIGHT)



#### E. SPECIAL FEATURES :

- a. LANGUAGE (ENGLISH/FRANÇAIS/ ESPAÑOL)
- b. SLEEP TIMER (OFF/30 MIN/60 MIN /90 MIN/120 MIN)
- c. WIDE FORMAT (NORMAL/WIDE/ZOOM)
- d. RESET ALL SETTING
- e. IMAGE CLEANER

## DTV Mode



#### A. DTV TUNER SETUP

- a. TIME ZONE:
  - 1.HAWALL
  - 2.EASTTERN TIME
  - 3.INDIANA
  - 4.CENTRAL TIME
  - 5.MOUNTAIN TIME
  - 6.ARIZONA
  - 7.PACIFIC TIME
  - 8.ALASKA

#### b. CABLE/AIR/AUTO

#### c. SCAN



#### d. MANUAL SCAN

##### SCAN MODE:

1. ADD-ON MODE
2. RANGE MODE
  - (1)FROM CHANNEL
  - (2)TO CHANNEL

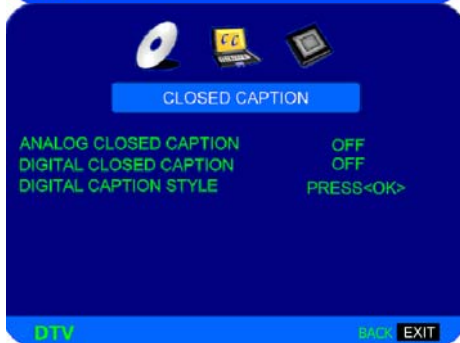


e. CHANNEL SKIP



f. DIGITAL AUDIO OUT

1. PCM
2. DOLBY DIGITAL
3. OFF



B.CLOSED CAPTION:

- a. ANALOG CLOSED CAPTION (OFF/YES)
- b. DIGITAL CLOSED CAPTION (OFF/YES)



c. DIGITAL CAPTION STYLE

- 1.AS BROADCASTER
- 2.CUSTOM
  - (1) FONT SIZE
    - α.LARGE
    - β.SMALL
    - γ.MEDIUM
  - (2) FONT COLOR
    - α .BLACK



$\beta$ .WHITE

$\gamma$ .GREEN

$\delta$ .BLUE

$\varepsilon$ .RED

$\zeta$ .CYAN

$\eta$ .YELLOW

$\theta$ .MAGENTA

(3) FONT OPACITY

$\alpha$ .SOLID

$\beta$ .TRANSLUCENT

$\gamma$ .TRANSPARENT

(4)BLACKGROUND COLOR

$\alpha$ .BLACK

$\beta$ .WHITE

$\gamma$ .GREEN

$\delta$ .BLUE

$\varepsilon$ .RED

$\zeta$ .CYAN

$\eta$ .YELLOW

$\theta$ .MAGENTA

(5) BLACKGROUND OPACITY

$\alpha$ .SOLID

$\beta$ .TRANSLUCENT

$\gamma$ .TRANSPARENT

(6) WINDOW COLOR

$\alpha$ .BLACK

$\beta$ .WHITE

$\gamma$ .GREEN

$\delta$ .BLUE

$\varepsilon$ .RED

$\zeta$ .CYAN

$\eta$ .YELLOW

$\theta$ .MAGENTA

(7) WINDOW OPACITY

$\alpha$ .SOLID

$\beta$ .TRANSLUCENT

$\gamma$ .TRANSPARENT



### C. PASSWORD

- PRESS<OK> , enter 0000
- get to "CHANNEL BLOCK", then press <OK>

### PIP table

Sub MAIN	AV1	AV2	AV3	COMPONENT 1	COMPONENT 2	HDMI*	RGB	TV	DTV
AV1	N	Y	Y	Y	Y	Y	Y	Y	Y
AV2	Y	N	Y	Y	Y	Y	Y	Y	Y
AV3	Y	Y	N	Y	Y	Y	Y	Y	Y
COMPONENT 1	Y	Y	Y	N	N	N	N	Y	N
COMPONENT 2	Y	Y	Y	N	N	N	N	Y	N
HDMI	Y	Y	Y	N	N	N	N	Y	N
RGB	Y	Y	Y	N	N	N	N	Y	N
TV	Y	Y	Y	Y	Y	Y	Y	N	Y
DTV	Y	Y	Y	N	N	N	N	Y	N

\* Sub/HDMI doesn't support 1080i.

## Chapter4      Factory preset timings

---

This timing chart is already preset for the analog & digital displays..

### 1. RGB PC preset modes

Mode No.	Resolution	Refresh Rate (Hz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Horizontal Sync Polarity (TTL)	Vertical Sync Polarity (TTL)	Pixel Rate (MHz)	Remark
1	640x480	60	31.5	59.94	N	N	25.175	Windows
2	640x480	75	37.5	75.00	N	N	31.500	Windows
3	720 x 400	70	31.46	70.08	N	P	28.320	DOS
4	800x600	60	37.9	60.317	P	P	40.000	Windows
5	800x600	75	46.9	75	P	P	49.500	Windows
6	800x600	85	53.7	85.06	P	P	56.250	Windows
7	Ⓢ1024x768	60	48.4	60.01	N	N	65.000	Windows
8	1024x768	70	56.5	70.07	N	N	75.000	Windows
9	1024x768	75	60.0	75.03	P	P	78.750	Windows
10	1280X1024	60	63.98	60.02	P	P	108.000	Windows

Remark: P: positive, N: negative      Ⓢ1024x768 @60 Hz: Primary

### 2. HDMI video digital preset modes

Mode No.	Resolution
1	480i
2	480p
3	720p
4	1080i

---

### 3. HDMI-DVI video preset modes

Mode No.	Resolution
1	480i
2	480p
3	720p
4	1080i

### 4. HDMI-DVI PC preset modes

Mode No.	Resolution	Refresh Rate (Hz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Horizontal Sync Polarity (TTL)	Vertical Sync Polarity (TTL)	Pixel Rate (MHz)	Remark
1	640x480	60	31.5	59.94	N	N	25.175	Windows

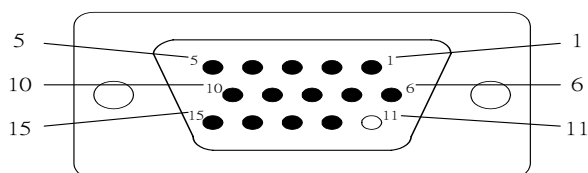
# Chapter 5 Pin Assignment

There are analog and digital connectors as video input source in this model.

## A. Input signal

### 1. RGB PC Connector

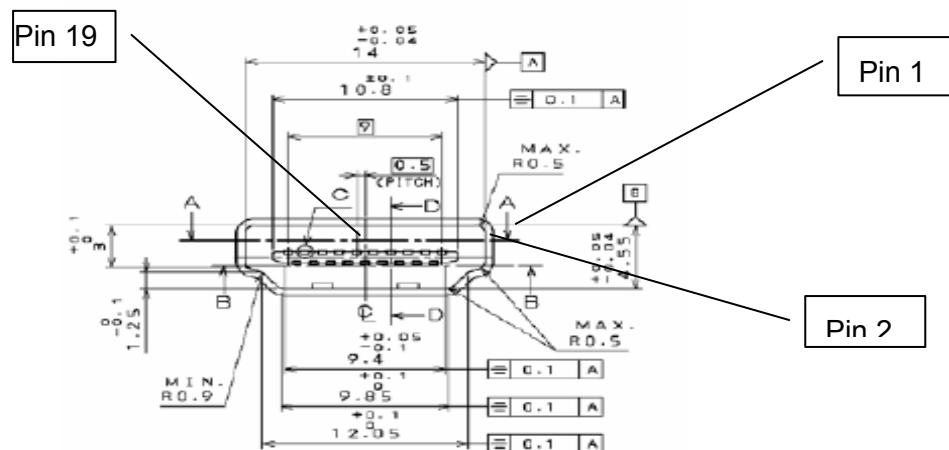
- a. Type: Analog
- b. Frequency: H: 30-80KHzV: 60-85Hz
- c. Signal level: 0.7Vp-p
- d. Impedance: 75Ω
- e. Synchronization H/V separate sync:  
H/V composite sync: Sync on Green  
TTL  
TTL
- f. Video bandwidth: 135MHz
- g. Connector type: 15-pin D-Sub, female



Pin Number	Pin Assignment	Pin Number	Pin Assignment
1	Red video input	9	+5V
2	Green video input	10	Ground
3	Blue video input	11	No connection
4	Ground	12	(SDA)
5	Ground	13	Horizontal sync (Composite sync)
6	Red video ground	14	Vertical sync
7	Green video ground	15	(SCL)
8	Blue video ground		

## 2. HDMI Connector

- a. Frequency:                      H: 15.734KHz                      V: 60Hz  
    H: 31KHz                      V: 60Hz  
    H: 45KHz                      V: 60Hz  
    H: 33KHz                      V: 60Hz
- b. Polarity:                      Positive or Negative
- c. Type:                      Type A
- d. Pin Assignment:              Please see below



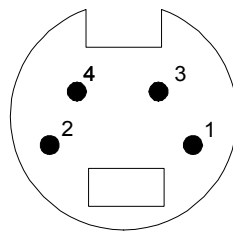
Pin	Signal Assignment	Pin	Signal Assignment
1	TMDS Data2+	2	TMDS Data2 Shield
3	TMDS Data2-	4	TMDS Data1+
5	TMDS Data1 Shield	6	TMDS Data1-
7	TMDS Data0+	8	TMDS Data0 Shield
9	TMDS Data0-	10	TMDS Clock+
11	TMDS Clock Shield	12	TMDS Clock-
13	CEC	14	Reserved (N.C. on device)
15	SCL	16	SDA
17	DDC/CEC Ground	18	+5V Power
19	Hot Plug Detect		

---

### 3. AV/Composite Video (CVBS) Connector

- a. Frequency:           H: 15.734KHz       V: 60Hz (NTSC)
- b. Signal level:       1Vp-p   Sync (H+V):0.3V below Video (Y+C)
- c. Impedance:         75Ω
- d. Connector type:    RCA jack

### 4. AV/S-Video Connector



1, 2 = GND  
3 = Luminance (Y)  
4 = Chrominance(C)

- a. Frequency:           H: 15.734KHz       V: 60Hz (NTSC)
- b. Signal level:       Y: 1Vp-p           C: 0.286Vp-p
- c. Impedance:         75Ω
- d. Connector type:     4-pin mini DIN

### 5. Component video Connector

- a. Frequency:       H: 15.734KHz       V: 60Hz (NTSC-480i)
- H: 31KHz       V: 60Hz (NTSC-480p)
- H: 45KHz       V: 60Hz (NTSC-720p)
- H: 33KHz       V: 60Hz (NTSC-1080i)
- b. Signal level:    Y: 1Vp-p
- Pb: ±0.350Vp-p   Pr: ±0.350Vp-p
- c. Impedance:       75Ω
- d. Connector type:  RCA jack

---

6. F-type TV RF connector

NTSC system

a. Signal level                      Analog 1Vp-p typical (45tdB~90dB)

b. Frequency                      55~801 MHz

ATSC system

a. IF-output level                  1Vp-p minimum

b. Frequency                      57~803 MHz

QAM system (supporting clear QAM)

a. IF-output level                  1Vp-p minimum

b. Frequency                      57~849 MHz

7. PC Stereo audio

a. Signal level:                      1Vrms

b. Impedance:                      47K $\Omega$

c. Connector type:                  3.5  $\phi$  mini jack

8. Video Stereo audio

a. Signal level:                      0.7Vrms

b. Impedance:                      47K $\Omega$

c. Frequency Response:          250Hz-20KHz

d. Connector type:                  RCA L/R:

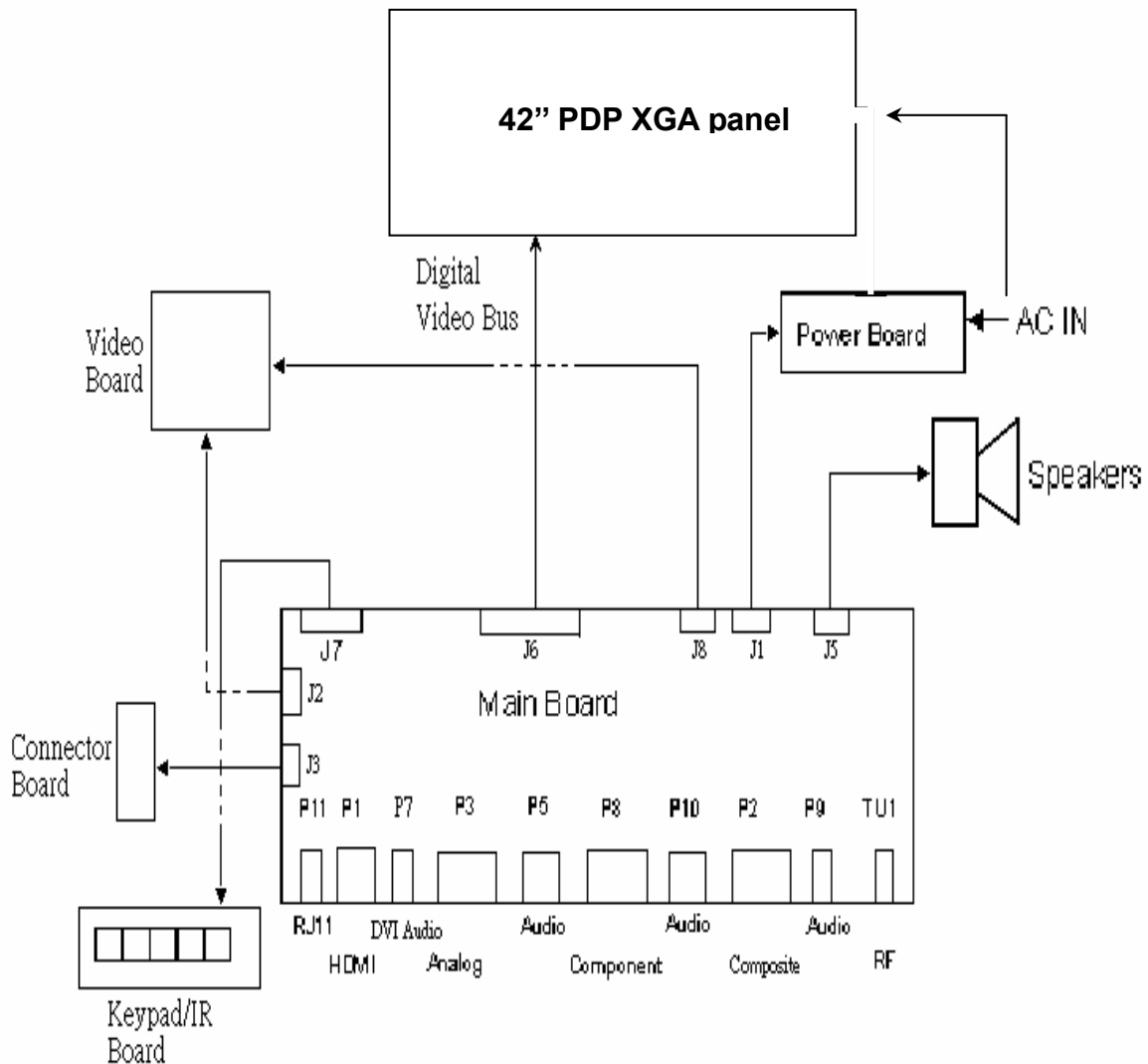
B. Output Signal

Output	Connector Type
ANALOG AUDIO OUT	Stereo RCA Jack x 2
DIGITAL AUDIO OUT	Optical x 1
Headphone	Mini jack x 1

- 
1. Analog Audio out
    - a. Signal level: 0.7Vrms
    - b. Impedance: 47K $\Omega$
    - c. Frequency Response: 250Hz-20KHz
    - d. Connector type: RCA L/R
  2. Digital audio out
    - a. Peak emission wave length: 630 – 690  $\mu$ m
    - b. Transmission Speed: 13.2M pbs
    - c. Connector type: Optical fiber transmitter
  3. Headphone
    - a. Signal level: 1Vrms (max.)
    - b. Impedance: 32 $\Omega$
    - c. Output: 50 mW
    - d. Connector type: Earphone mini jack

## Chapter 6 Block Diagram

### System Block Diagram



The TV system block diagram is powered by power board that transforms AC source of 100V~240V AC +/- 10% @ 50/60 HZ into system request power source. The main board receives different types of video signal into the MTK8205 Ic. Afterward, the MTK8205 Ic process the signals control the various functions of the monitor and outputs control signal, video signal and power to the 42" PDP XGA panel to be displayed.

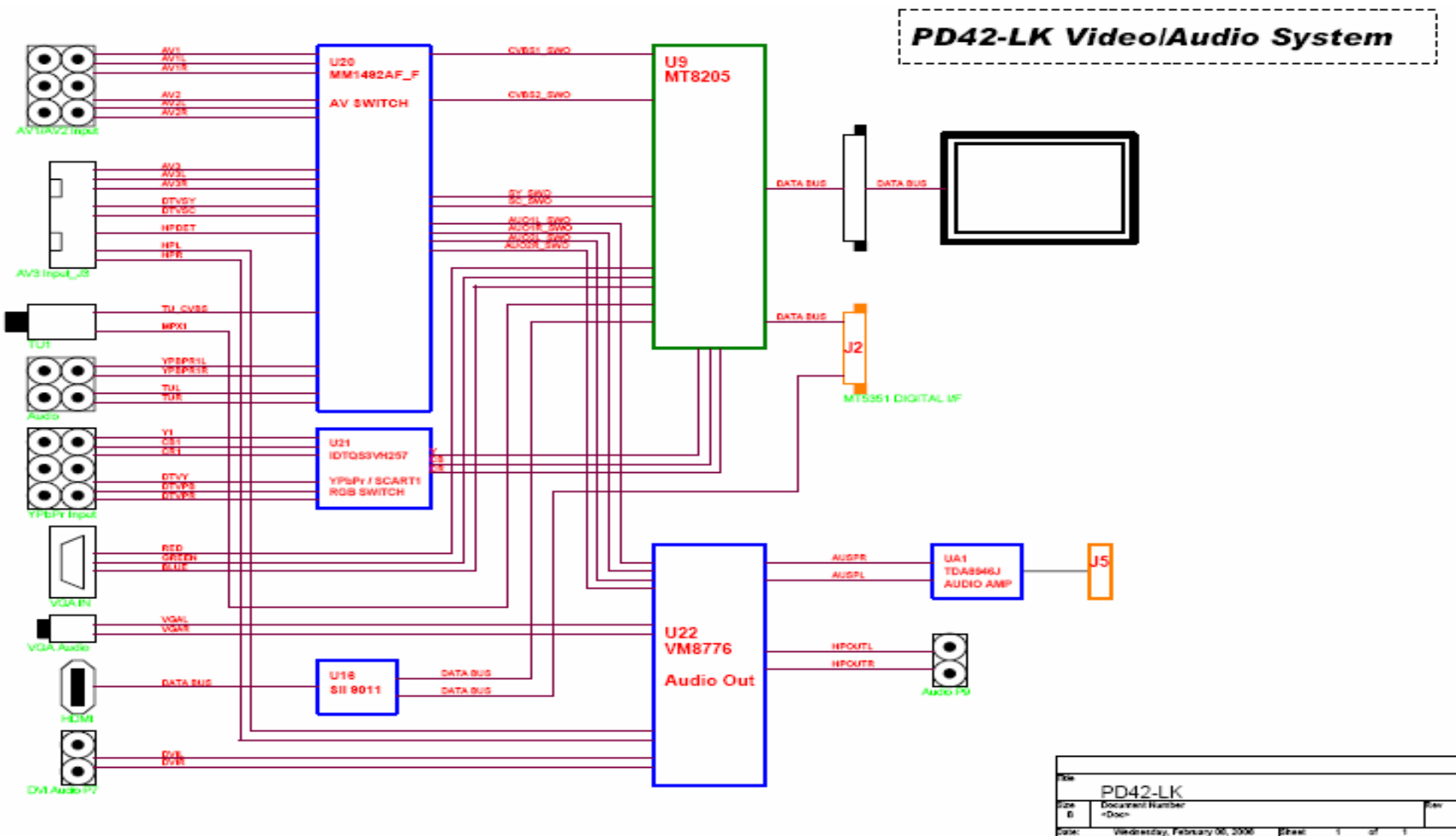
---

The analog video signals of S-video, YPbPr, TV, PC and A/V all video signals are translated from analog signals into MTK8205 generates the vertical and horizontal timing signals for display device.

The analog audio of s-video, YPbPr, TV, PC and A/V is transmitting to the WM8776 processed. The purpose is process the input audio signal to control volume, bass, treble, surround, and balance. The HDMI video and audio is must transmitting to sil9011 processed then TMDS signal to the MTK8205 generates the vertical and horizontal timing signals for display device.

The DTV signal is processes to the tuner and output to MT5111 who handle ATSC input to match MPEG-2 package, then transfer to MT5351. After passing through decoder, the signal will be with the digital signal tri-dtate from HDMI transfer to digital port of MT8205 . All functions are controllable by the main board. Plus, all functions in the IC boards are programmable using I2C Bus.

## Main Board Block Diagram

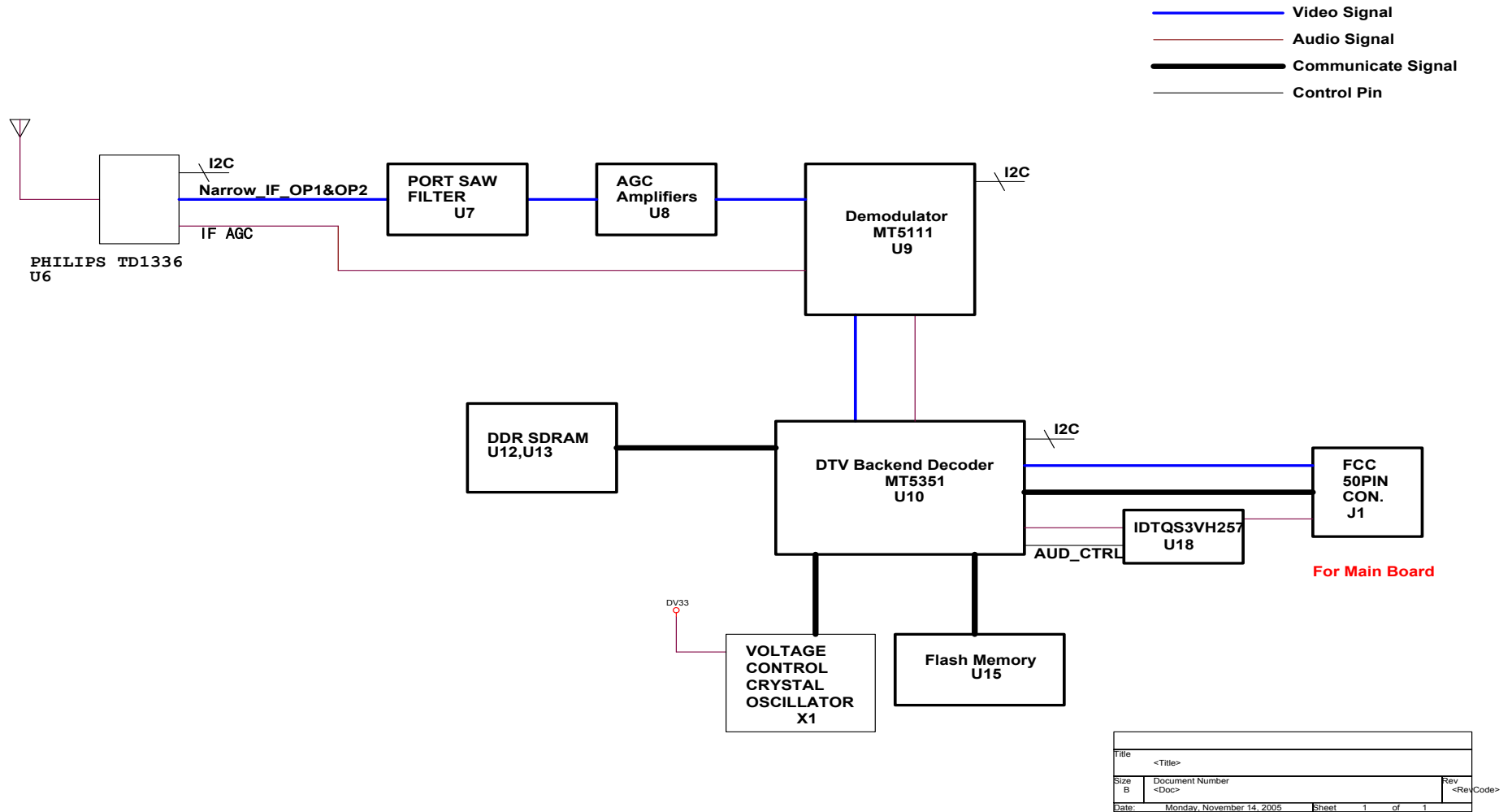


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Page 6-3

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## Video Board Block Diagram



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Page 6-4

File No. SG-0184

## Chapter7 Main Board I/o Connections

---

### J7 CONNECTION (TOP→BOTTOM)

Pin	Description
1	“Auto”
2	“Left”
3	“Right”
4	“Down”
5	“Gnd”
6	“Up”
7	“Menu”
8	“Source”
9	“Power”
10	“LED”
11	“IR”
12	“+5V”

### J1 CONNECTION (TOP→BOTTOM)

Pin	Description
1	“POWRSW”
2	“+12V”
3	“+12V”
4	“+12V”
5	“GND”
6	“GND”
7	“GND”
8	“GND”
9	“+5V”
10	“+5V”
11	“+5V”
12	“RLY_ON”
13	“VS_ON”

---

### J3 CONNECTION (TOP→BOTTOM)

Pin	Description
1	"SVDET2#"
2	"S1C_GND"
3	"S1C_IN"
4	"S1Y_GND"
5	"S1Y_IN"
6	"AGND"
7	"AV3R"
8	"AV3R GND"
9	"AV3L "
10	"AV3_GND"
11	"AV3_IN"
12	"AV3L GND"
13	"HPL "
14	"HPDET#"
15	"HPR"
16	"GNDV"

---

J2 CONNECTION (TOP→BOTTOM)

Pin	Description	Pin	Description
1	"GND"	26	"GND"
2	"I2C_SW"	27	"VOG3"
3	"OREQUEST#"	28	"VOG2"
4	"OREADY#"	29	"VOG1"
5	"ORESET#"	30	"VOG0"
6	"GND"	31	"GND"
7	"VOPCLK"	32	"VOB7"
8	"VODE"	33	"VOB6"
9	"VOVSYNC"	34	"VOB5"
10	"VOHSYNC"	35	"VOB4"
11	"GND"	36	"GND"
12	"VOR7"	37	"VOB3"
13	"VOR6"	38	"VOB2"
14	"VOR5"	39	"VOB1"
15	"VOR4"	40	"VOB0"
16	"GND"	41	"GND"
17	"VOR3"	42	"AO1SDATA0"
18	"VOR2"	43	"AO1LRCK"
19	"VOR1"	44	"AO1BCK"
20	"VOR0"	45	"AO1MCLK"
21	"GND"	46	"GND"
22	"VOG7"	47	"U2RX"
23	"VOG6"	48	"U2TX"
24	"VOG5"	49	"U0RX"
25	"VOG4"	50	"U0TX"

---

J8 CONNECTION (TOP→BOTTOM)

Pin	Description
1	“+5V”
2	“GND”
3	“GND”
4	“+12V”
5	“+12V”

# Chapter 8      Theory of Circuit Operation

---

## **The operation of D-SUB 15pin route**

The D-SUB 15pin is input analog signal to the MTK8205 transfer A/D converter then generates the vertical and horizontal timing signals for display device.

## **The operation of HDMI CON route**

The HDMI CON is input digital signal the signal is process to the sil9011. Then transfer to the MTK8205, the MTK8205 generates the vertical and horizontal timing signals for display device.

## **The operation of HDTV & Component route**

HDTV & Component signal is input to switch IDTQS3VH257 (Select Component1 or 2). Then transfer to the MTK8205 the MTK8205 generates the vertical and horizontal timing signals for display device.

## **The operation of Video 1,2,3 & S-Video route**

The Video 1,2,3 and S-Video signal is transmission signal to main board MM1492 (Switch) and output to MTK8205 the MTK8205 generates the vertical and horizontal timing signals for display device.

## **The operation of TV route**

TV signal is processes to the tuner and output to MM1492 (switch) then transfer to MTK8205 the MTK8205 generates the vertical and horizontal timing signals for display device. Audio is processes to the tuner output to SIF circuit and output to MTK8205. Then MTK8205 process to wm8776 and output to TDA8946J transfer to speaker

## **The operation of DTV route**

DTV signal is processes to the tuner and output to MT5111 who handle ATSC input to match MPEG-2 package, then transfer to MT5351. After passing through decoder, the signal will be with the digital signal tri-dtate from HDMI transfer to digital port of MT8205

## **The operation of keypad**

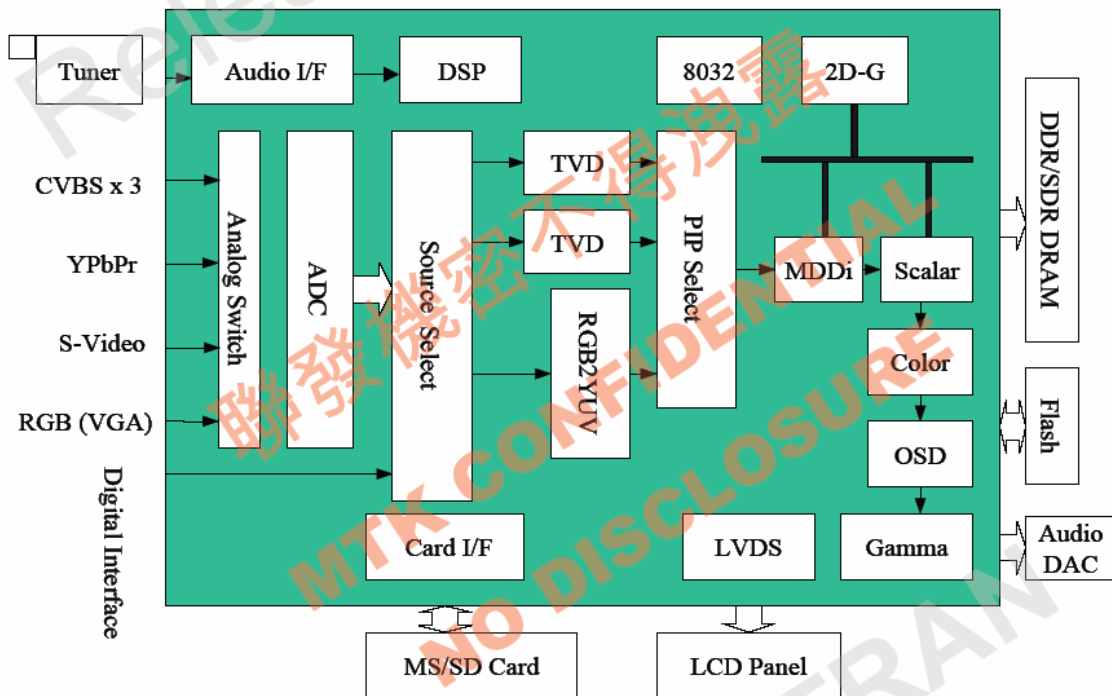
There are 7 keys to control and select the function of P42 and also has one LED to indicate the status of operation. They are "Power, Menu, CH+, CH-, VOL+ ,VOL - , Input".

- 
1. The power key through POW and GND to control MTK8205, MTK8205 will receive a low signal to turn on or off system while press the power key.
  2. The other key the same as power key .
  3. The LED is constructed with two separate LED which color is **green** and orange. The MTK8205 direct control the LED's when MTK8205 (OGO5) is low the LED is orange (Close power) when MTK8205 (OGO5) is high the LED is **green** (Open power).

### **MT8205 Application**

MT8205 is a highly integrated single chip for **PDP** TV supporting video input and output format up to HDTV. It includes 3D comb filter TV Decoder to retrieve the best image from popular composite signals. On-chip advanced motion adaptive de-interlacer converts accordingly the interlace video into progressive one with overlay of a 2D Graphic processor. Optional 2nd HDTV or SDTV inputs allows user to see multi-programs on same screen. Flexible scalar provides wide adoption to various **PDP** panel for different video sources. Its on-chip audio processor decodes analog signals from Tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor reduces the system BOM and shortens the schedule of UI design by high level C program. MT8205 is a cost-effective and high performance HDTV-ready solution to TV manufactures.

## BOLOCK DIAGRAM



### 1. Video input

#### a. Input Multiplexing

- 1.component X2
- 2.composite X3
- 3.s-videoX1
- 4.HDMI X1
- 5.VGA X1
- 6.RF X2

---

b. Input formats:

- 1.support HDTV 480i/480p/720p/1080i
- 2.support Y/C signal 1VP-P/75Ω
- 3.support Y/C signal 1VP-P/75Ω
- 4.support 480i/408p/720p/1080i
- 5.support VGA input up to 1280x1024@60HZ
- 6.support NTSC system Frequency 55~801MHZ
7. support ATSC system Frequency 57~863MHZ

## 2. TV Decoder

For pip/pop:

Dual identical TVD on chip

3D-comb for both path

Dual VBI decoders for the application of V-chip

## 3. Support Formats:

Support NTSC, NTSC-4.43

Support ATSC

Automatic Luma / Chroma gain control

Automatic TV standard detection

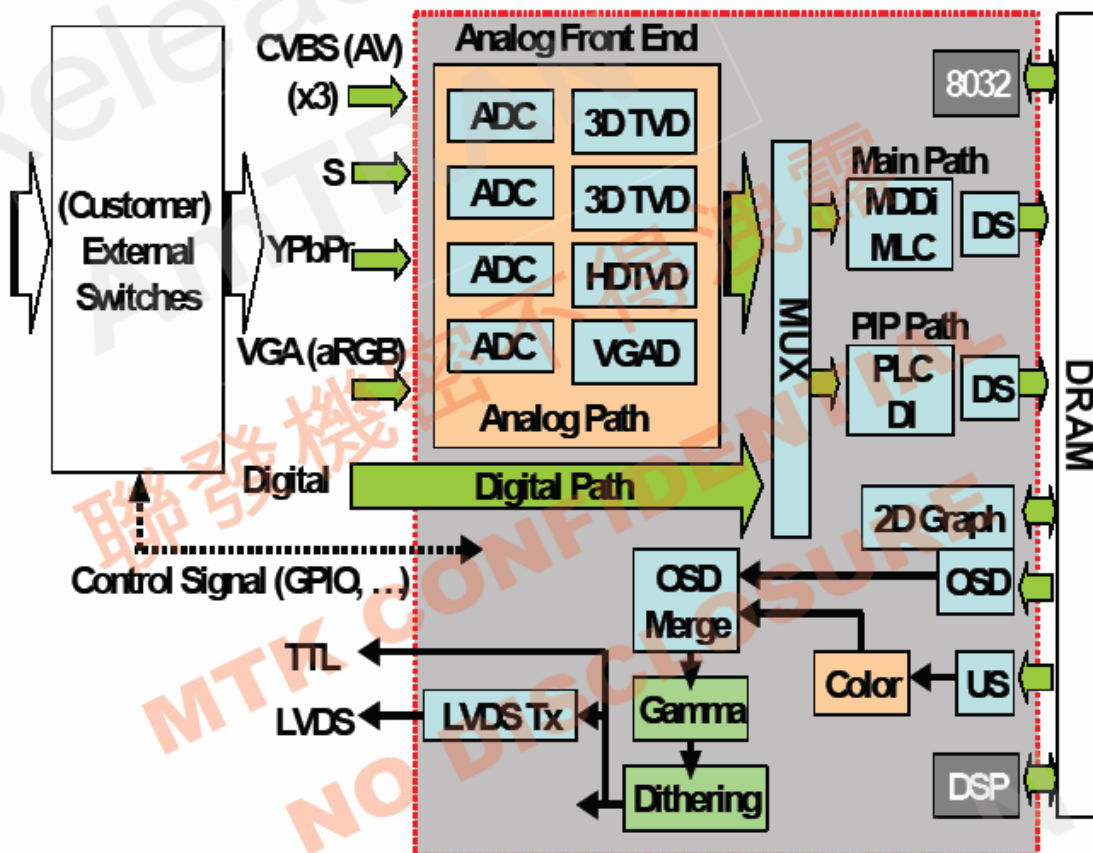
NTSC Motion Adaptive 3D comb filter

Motion adaptive 3D Noise Reduction

VBI decoder for closed-caption/XDS/Teletext/WSS/VPS

Macro vision detection

## BOLOCK DIAGRAM



### 4. 2D-Graphic/OSD processor

Two OSD planes.

Support alpha blending among these two planes and video

Support text/bitmap decoder

Support line/rectangle/gradient fill

Support bitblt

Support color key function

Support clip mask

65535/256/16/4/2-color bitmap format OSD

Automatic vertical scrolling of OSD image

Support OSD mirror and upside down

---

## 5. Microprocessor interface

When power is supplied and power key is pressed then the rest circuit lets Reset to low state that will reset the MTK8205 to initial state. After that the Reset will transits to high state and the MTK8205 start to work that microprocessor executes the programs and configures the internal registers. The execution speed of CPU is 133 MHz.

a. The I/O ports are configured as follows :

Pin name	Function	Type	Description
AF26	VGASCL	Input / Output	
AE26	VGASDA	Input / Output	
AB23	REQUEST#	Input / Output	
AB24	READY#	Input / Output	
AD22	SCL	Input / Output	
AC22	SDA	Input / Output	
OBO0	SOURCE	Input	Key detection
OBO1	MENU	Input	Key detection
OBO2	UP	Input	Key detection
OBO3	DOWN	Input	Key detection
OBO4	RIGHT	Input	Key detection
OBO5	LEFT	Input	Key detection
OBO6	AUTO	Input	Key detection
OBO7	POWER	Input	Key detection
OGO5	LED	Output	
AF24	IR	Input / Output	
AE23	GPIO	Output	Power on of TV board and panel
AD23	PWM0	Output	Backlight Adjustmance
AC23	PWM1	Output	Select mute
AF6	ORO6	Output	RCA out mute
AE20	UP1_4	Input	S-video Detect
AF20	UP1_3	Output	HDMI SCDT
AE19`	UP1_2	Output	YCBCRSEL
AE21	UP3_0	Output	Backlight ON/OFF
AD21	UP3_1	Output	HDMI CAB

---

**b. PIP/POP HARDWARE LIMITATION:**

		<b>Secondary Window Source</b>								
<b>Primary Window Source</b>		<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>E</b>	<b>F</b>	<b>G</b>	<b>H</b>	<b>I</b>
<b>ATSC Tuner</b>	<b>A</b>	X	✓	✓	✓	✓	X	X	X	X
<b>NTSC Tuner</b>	<b>B</b>	✓	X	✓	✓	✓	✓	✓	✓	✓
<b>A/V1</b>	<b>C</b>	✓	✓	X	✓	✓	✓	✓	✓	✓
<b>A/V2</b>	<b>D</b>	✓	✓	✓	X	✓	✓	✓	✓	✓
<b>A/V3 (Side)</b>	<b>E</b>	✓	✓	✓	✓	X	✓	✓	✓	✓
<b>Analog HD1 (480i~1080i)</b>	<b>F</b>	X	✓	✓	✓	✓	X	X	X	X
<b>Analog HD2 (480i~1080i)</b>	<b>G</b>	X	✓	✓	✓	✓	X	X	X	X
<b>Digital HD1 (HDMI)</b>	<b>H</b>	X	✓	✓	✓	✓	X	X	X	X
<b>RGB</b>	<b>I</b>	X	✓	✓	✓	✓	X	X	X	X

**Input Matrix for Windowing Functionality**

**6. Video processor**

**a. Color management**

Flesh tone and multiple-color enhancement  
Gamma/anti-Gamma correction  
Color Transient Improvement (CTI)  
Saturation/hue adjustment  
Contrast/Brightness/Sharpness Management  
Sharpness and DLTI/DCTI  
Brightness and contrast adjustment  
Black level extender  
White peak level limiter  
Adaptive Luma/Chroma Management

**b. De-interlacing**

Automatic detect film or video source  
3:2/2:2 pull down source detection  
Advanced Motion adaptive de-interlacing

---

### c. Scaling

Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X

Advanced linear and non-linear Panorama scaling

Programmable Zoom viewer

Picture in picture (PIP)

Picture in picture

### d. Display

12/10 10/8 8/6 Dithering processing for PDP display

10bit gamma correction

Support Alpha blending for Video and two OSD panel

Frame rate conversion

## 7. DRAM Usage

8205,2pcs of 8X16 DDR166 is necessary

Here is a comparison chart between (2XDDR)and(1XDDR)

	DDR*1(16Mb)	DDR*2(32Mb)
NR	Y	Y
3D-Comb	Y	Y
MDDi	480i/576i	1080i
PIP	*Y	Y
POP	*Y	Y
Display	1024x768	1920x1080

MTK8205 8MX16 DDRAM test report

Item	Brand	IC Number	Speed	Voltage	Package	Result
1	ESMT	M13S128168A-6T	6T	2.5V	TSOP66	Pass
2	elixir	N2DS12H16CT-6K	6T	2.5V	TSOP66	Pass
3	Hynix	HY5DU281622AT-6	6T	2.5V	TSOP66	Pass
4	ProMos	V58C2128164SBT6	6T	2.5V	TSOP66	Pass

## 8. Flash Usage

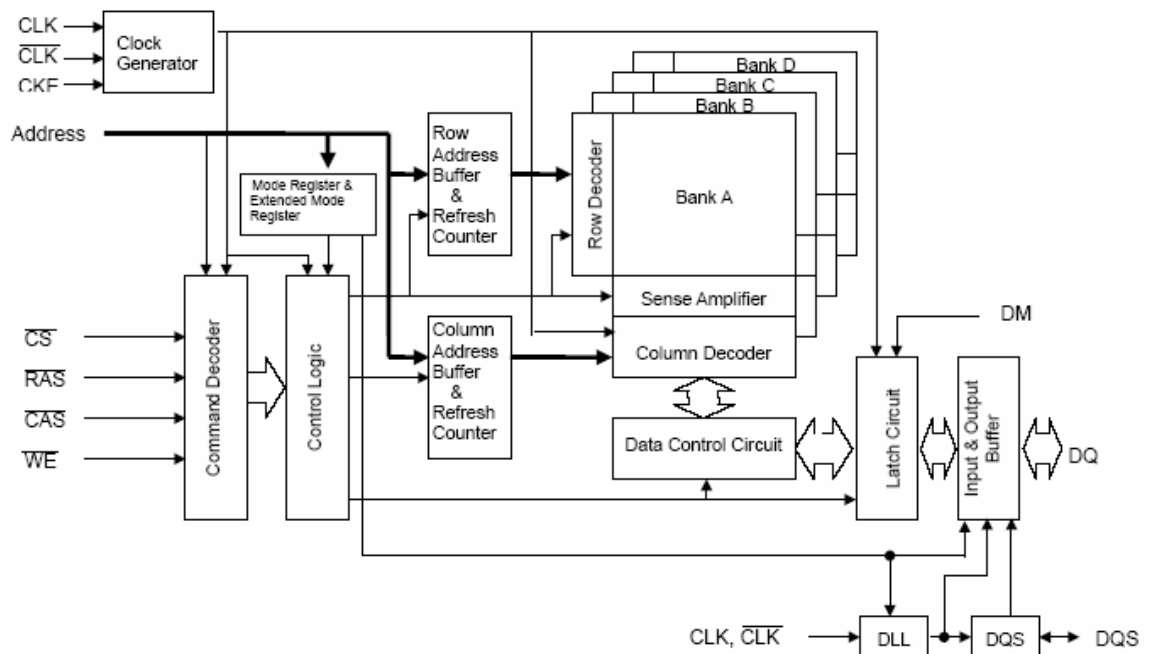
Flash is used to store FW code, fonts, bitmaps, and big tables for VGA, Video, and Gamma  
2Mbyte is recommended to build a general TV model

MTK8205 Flash ROM support test report

Item	Brand	IC Number	Speed	Size	Voltage	Package	Result
1	MXIC	29LV800ABTC-70	70ns	8Mb	3.3V	TSOP48	Pass
2	MXIC	29LV800ATTC-70	70ns	8Mb	3.3V	TSOP48	Pass
3	MXIC	29LV800ATTI-70	70ns	8Mb	3.3V	TSOP48	Pass
4	MXIC	29LV800BTC-55	55ns	8Mb	3.3V	TSOP48	Pass
5	MXIC	29LV800TTC-70	70ns	8Mb	3.3V	TSOP48	Pass
6	MXIC	29LV160BBTC-70	70ns	16Mb	3.3V	TSOP48	Pass
7	MXIC	29LV160BTTC-70	70ns	16Mb	3.3V	TSOP48	Pass
8	MXIC	26LV160BTC-70	70ns	16Mb	3.3V	TSOP48	Pass
9	Fujitsu	29LV800BA-70PFTN	70ns	8Mb	3.3V	TSOP48	Pass
10	Fujitsu	29LV800TA-70PFTN	70ns	8Mb	3.3V	TSOP48	Pass
11	Fujitsu	29LV800TA-90PFTN	90ns	8Mb	3.3V	TSOP48	Pass
12	Fujitsu	29LV160BE-70PFTN	70ns	16Mb	3.3V	TSOP48	Pass
13	Fujitsu	29LV160TE-70PFTN	70ns	16Mb	3.3V	TSOP48	Pass
14	ST	M29W800AT-90N1	90ns	8Mb	3.3V	TSOP48	Pass
15	ST	M29W800AT-90N6	90ns	8Mb	3.3V	TSOP48	Pass
16	ST	M29W800DT-70N1	70ns	8Mb	3.3V	TSOP48	Pass
17	ST	M29W160EB-70N6	70ns	16Mb	3.3V	TSOP48	Pass
18	ST	M29W160ET-70N6	70ns	16Mb	3.3V	TSOP48	Pass
20	SST	39VF088-70-4C-EK	70ns	8Mb	3.3V	TSOP48	Pass
23	AMD	AM29LV160DT-70EC	70ns	16Mb	3.3V	TSOP48	Pass
24	ATMEL	AT49BV162A-70TI	70ns	16Mb	3.3V	TSOP48	Pass

## DDR SDRAM (M13S128168A-6T) Application

Functional Block Diagram



## Pin description

Pin Name	Function	Pin Name	Function
A0~A11, BA0,BA1	Address inputs - Row address A0~A11 - Column address A0~A8 A10/AP : AUTO Precharge BA0, BA1 : Bank selects (4 Banks)	LDM, UDM	DM is an input mask signal for write data. LDM corresponds to the data on DQ0~DQ7; UDM correspond to the data on DQ8~DQ15.
DQ0~DQ15	Data-in/Data-out	CLK, $\overline{\text{CLK}}$	Clock input
$\overline{\text{RAS}}$	Row address strobe	CKE	Clock enable
$\overline{\text{CAS}}$	Column address strobe	$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable	$V_{\text{DDQ}}$	Supply Voltage for GDQ
$V_{\text{SS}}$	Ground	$V_{\text{SSQ}}$	Ground for DQ
$V_{\text{DD}}$	Power	$V_{\text{REF}}$	Reference Voltage for SSTL-2
LDQS, UDQS	Bi-directional Data Strobe. LDQS corresponds to the data on DQ0~DQ7; UDQS correspond to the data on DQ8~DQ15.	NC	No connection

## Command Truth Table

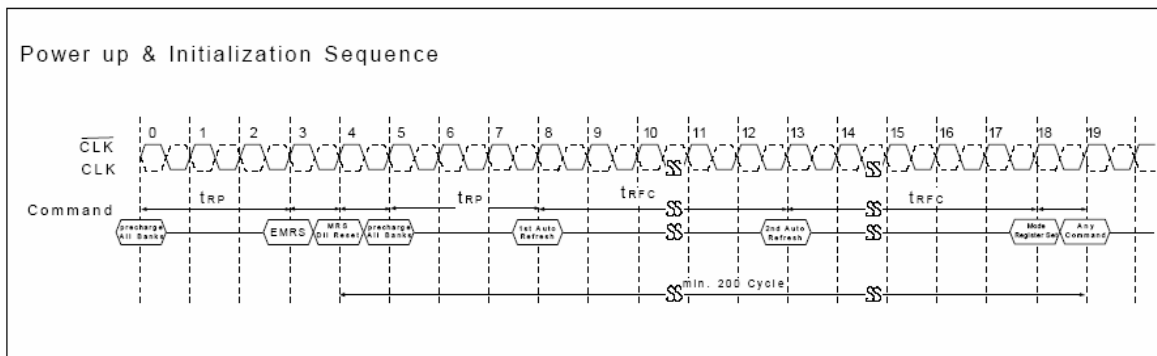
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0,1	A10/AP	A11, A9~A0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	H	H	X	X	X	X	3		
											3		
											3		
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address	4
	Auto Precharge Enable										H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge Power Down Mode		Exit	L	H	X	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X			8
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

### 1. Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

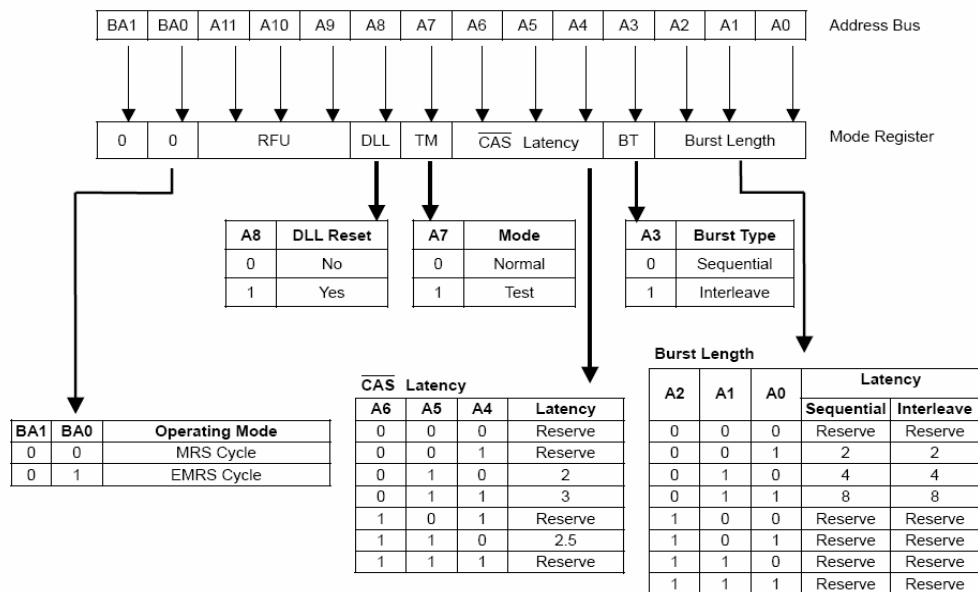
1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
  - Apply VDD before or at the same time as VDDQ.
  - Apply VDDQ before or at the same time as VTT & VREF).
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock (CLK, CLK), apply NOP & take CKE high.
4. Issue precharge commands for all banks of the device.
5. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)

6. Issue a mode register set command for “DLL reset”. The additional 200 cycles of clock input is required to lock the DLL.(To issue DLL reset command, provide “High” to A8 and “Low” to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command with low to A8 to initialize device operation.



## 2. Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on CS , RAS , CAS , WE and BA0 (The DDR SDRAM should be in all bank recharge with CKE already high prior to writing into the mode register). The state of address pins A0~A11 in the same cycle as CS , RAS , CAS , WE and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0~A2, addressing mode uses A3, CAS latency (read latency from column address) uses A4~A6. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



### 3. Precharge

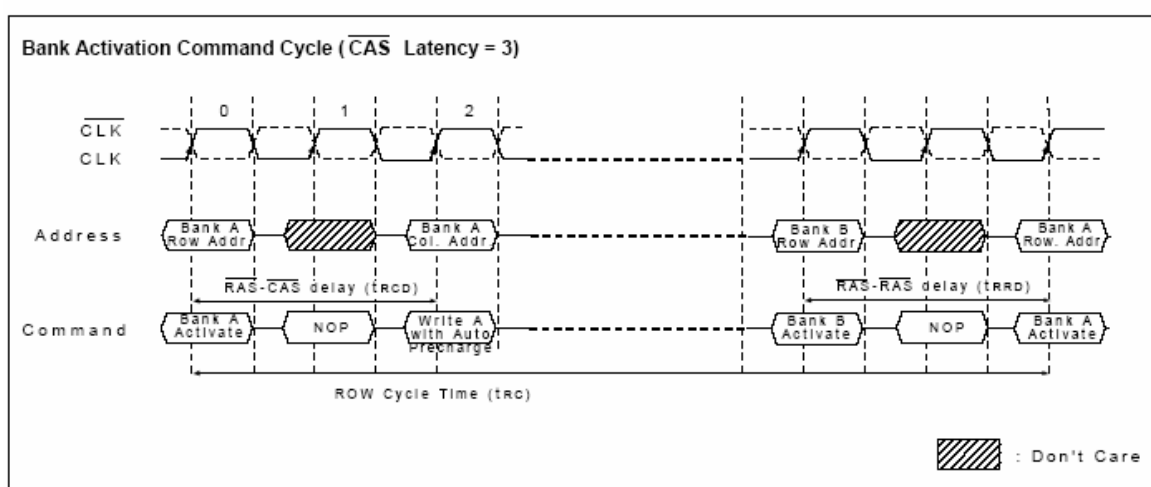
The precharge command is used to precharge or close a bank that has activated. The precharge command is issued when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle,  $t_{WR}(\text{min.})$  must be satisfied until the precharge command can be issued. After  $t_{RP}$  from the precharge, an active command to the same bank can be initiated.

Burst Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

#### 4. Row Active

The Bank Activation command is issued by holding CAS and WE high with CS and RAS low at the rising edge of the clock (CLK). The DDR SDRAM has four independent banks; so two Bank Select addresses (BA0, BA1) are required. The Bank Activation command to the first read or write command must meet or exceed the minimum of RAS to CAS delay time ( $t_{RCD}$  min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation command (Bank A to Bank B and vice versa) is the Bank-to-Bank delay time ( $t_{RRD}$  min).



#### 5. Read Bank

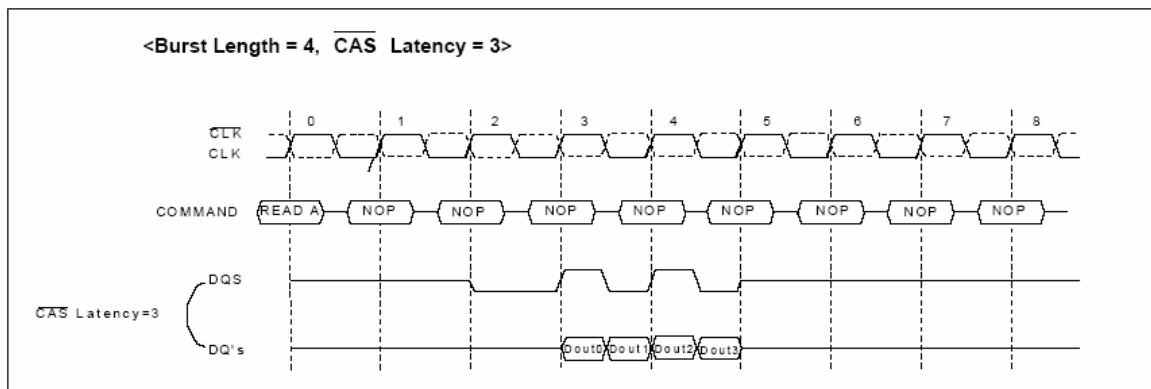
This command is used after the row activates command to initiate the burst read of data. The read command is initiated by activating CS, CAS, and deasserting WE at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

#### 6. Write Bank

This command is used after the row activates command to initiate the burst write of data. The write command is initiated by activating CS, CAS, and WE at the same clock sampling (rising) edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

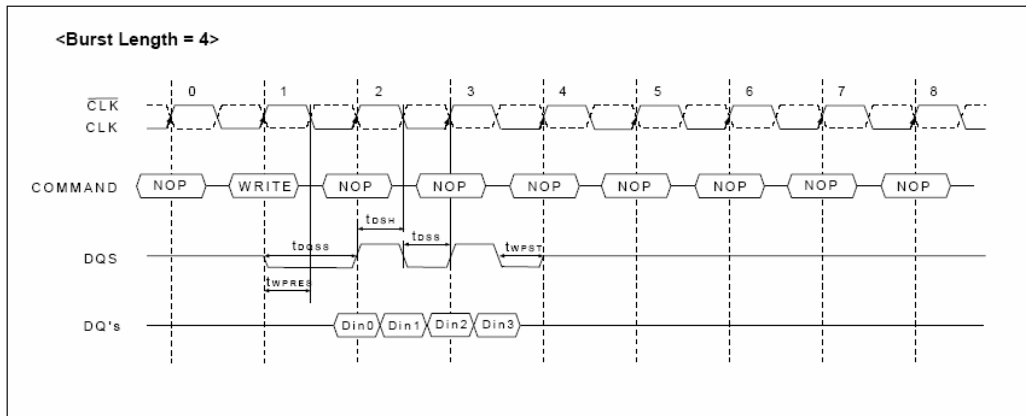
## 7. Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting CS and CAS low while holding RAS and WE high at the rising edge of the clock (CLK) after tRCD from the bank activation. The address inputs determine the starting address for the Burst, The Mode Register sets type of burst. (Sequential or interleave) and burst length (2, 4, 8). The first output data is available after the CAS Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by DDR SDRAM until the burst length is completed.



## 8. Burst Write Operation

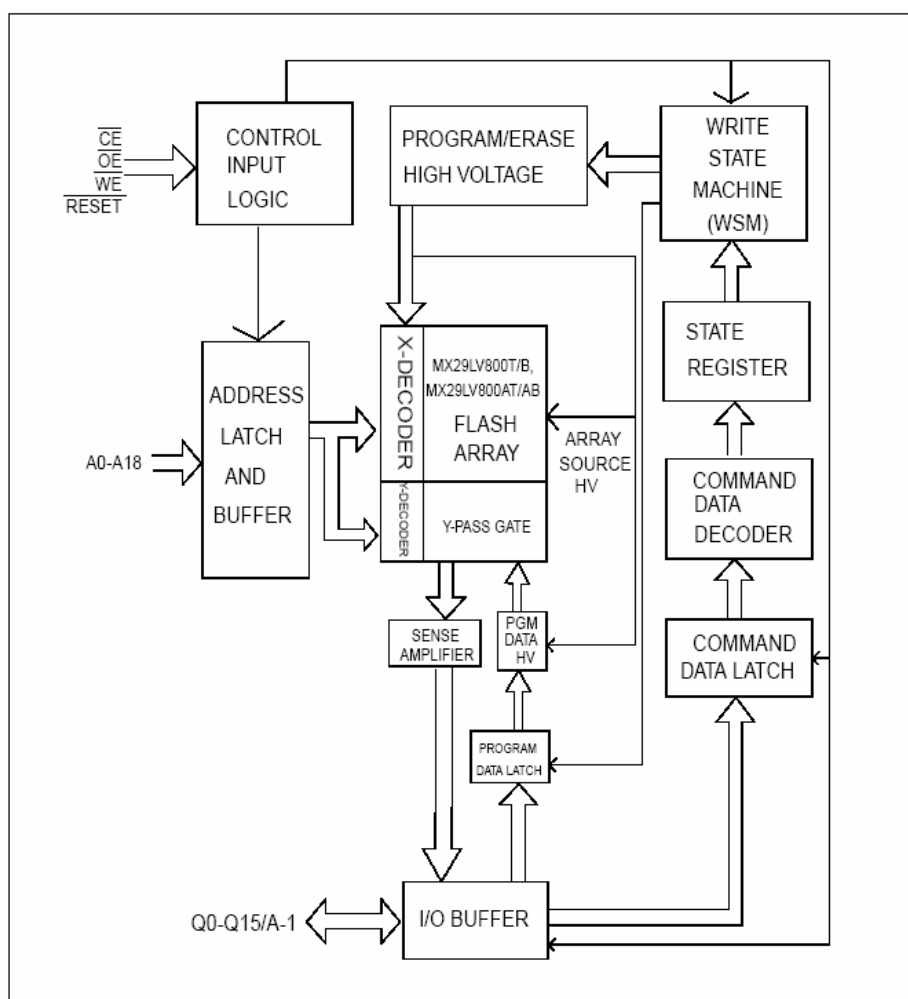
The Burst Write command is issued by having CS, CAS and WE low while holding RAS high at the rising edge of the clock (CLK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS (Data-in setup time) prior to data strobe edge enabled after tDQSS from the rising edge of the clock (CLK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.



### MX29LV160BTTC (Flash) Application

The MX29LV800T/B & MX29LV800AT/AB is a 8-mega bit Flash memory organized as 1M bytes of 8 bits or 512K words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV800T/B & MX29LV800AT/AB is packaged in 44-pin SOP, 48-pin TSOP, and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

## BLOCK DIAGRAM



### 1. COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

**TABLE 6. MX29LV800T/B & MX29LV800AT/AB BUS OPERATION**

DESCRIPTION	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	ADDRESS									Q0~Q7	Q8-Q15	
				A18 A12	A10 A11	A9	A8 A7	A6	A5 A2	A1	A0	BYTE =VIH		BYTE =VIL	
Read	L	L	H	AIN									Dout	Dout	=High Z DQ15=A-1
Write	L	H	L	AIN									DIN(3)	DIN	
Reset	X	X	X	X									High Z	High Z	High Z
Temporary sector unlock	X	X	X	AIN									DIN	DIN	High Z
Output Disable	L	H	H	X									High Z	High Z	High Z
Standby	Vcc ± 0.3V	X	X	X									High Z	High Z	High Z
Sector Protect	L	H	L	SA	X	X	X	L	X	H	L	DIN	X	X	
Sector Unprotected	L	H	L	X	X	X	X	H	X	H	L	DIN	X	X	
Sector Protection Verify	L	L	H	SA	X	VID	X	L	X	H	L	CODE(5)	X	X	

**NOTES:**

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 5.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 5 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H/XX00H means unprotected.  
Code=01H/XX01H means protected.
6. A18~A12=Sector address for sector protect.
7. The sector protect and chip unprotected functions may also be implemented via programming equipment.

## 2. WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory, the system must drive WE and CE to VIL, and OE to VIH. The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four. The "byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences. An erase operation can erase one sector, multiple sectors, or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Figure 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the auto select command sequence, the device enters the auto select mode. The system can then read auto select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Auto select Mode and Auto select Command Sequence section for more information. ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

Figure 1

Sector	Sector Size		Address range		Sector Address						
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000h-0FFFFh	00000h-07FFFh	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
SA15	32Kbytes	16Kwords	F0000h-F7FFFh	78000h-7BFFFh	1	1	1	1	0	X	X
SA16	8Kbytes	4Kwords	F8000h-F9FFFh	7C000h-7CFFFh	1	1	1	1	1	0	0
SA17	8Kbytes	4Kwords	FA000h-FBFFFh	7D000h-7DFFFh	1	1	1	1	1	0	1
SA18	16Kbytes	8Kwords	FC000h-FFFFFh	7E000h-7FFFFh	1	1	1	1	1	1	X

### 3. READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered. If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

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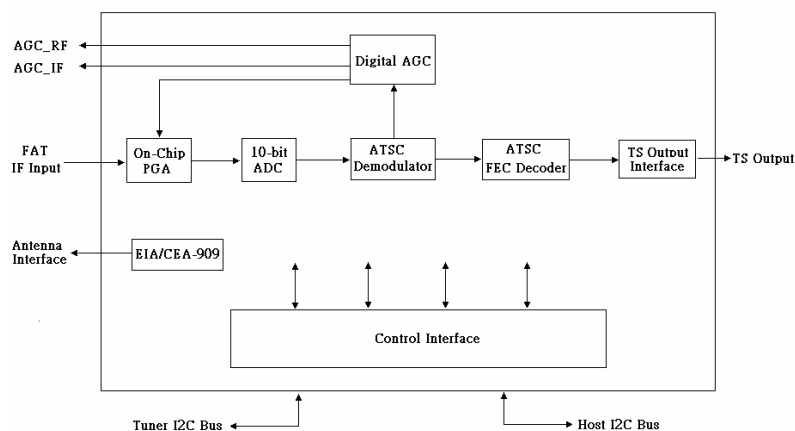
#### **4. READING ARRAY DATA**

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm. After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the auto select mode. See the "Reset Command" section, next.

#### **5. RESET COMMAND**

Writing the reset command to the device resets the device to reading array data. Addresses bits are don't care for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend). If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

## MT5111 Application:



MT5111 Functional Block Diagram

MT5111 is fully integrated single-chip 8-VSB , designed specifically for the digital terrestrial. HDTV receivers . The chip is fully compliant with the ATSC A/53 digital TV standard.

MT5111 includes a 10-bit A/D converter , 8-VSB demodulator , TCM(Trellis-Coded Modulation).

Decoder . and Reed-Solomon Forward Error Correction decoder . Moreover , an internal controller handles the acquisition and tracking to ensure the best receiving performance . The internal controller communicates with the external host controller via the I2C-compatible interface , and also provides direct control to the RF tuner via the second I2C-compatible interface.

MT5111 accepts either the direct IF signals centered at 44MHZ or 43.75MHZ , or the low IF signal Centered at 5.38MHZ . The center frequency of the incoming IF signal can also be programmed to other frequencies for Various applications . An On-chip programmable gain-controlled amplifier is designed to provide sufficient signal amplitude when the received RF signal is weak . The If signal is first sampled by a 10-bit A/D converter . Afterward , the digitized samples are further processed for adjacent channel interference rejection.

MT5111 measures the power level of the digitized sequence , and feeds the control voltages back to the RF tuner and the IF amplifier respectively . The control voltages are converted to analog signals through the on-chip 1-bit sigma-delta D/A converters plus the off-chip R-C low-pass filters . The automatic gain control keeps the received power level at a desired level and maximizes the received SNR .

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The carrier frequency offset and symbol timing offset are both estimated and compensated by a fully digital synchronizer . The synchronizer also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset . All synchronization in MT5111 are integrated in digital circuits , no external VCXO is required.

The equalizer is adopted to cancel the effect of multi-path fading channel during signal propagation in the air . The equalizer is not only capable of acquiring correct coefficients combination by specified adaptive algorithms , but also programmable to different configurations for various channel conditions.

The following FEC decoder corrects most of the errors by the concatenation of TCM and Reed-Solomon decoders . The on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: equalizer output , TCM decoder , and transport stream packets . The chip finally outputs the decoded MPEG-2 packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal , MT5111 also provides the capability to remove the NTSC co-channel interference. To achieve the best reception condition , an antenna interface compliant with EIA/CEA-909 is designed to control the antenna parameters.

MT5111 is designed with efficient mechanisms of power saving . When configured to enter the sleep mode by the system host , it can immediately turn off almost all embedded hardware except the on-chip controller to reduce the power consumption . Resuming from sleep mode is also triggered by the system host . Upon returning to the operation mode , the chip will try to re-acquire the DTV signal automatically.

#### MT5111 Key Features:

1. ATSC compliant 8-VSB demodulator
2. Accepts direct IF (44 MHz or 43.75 MHz) and low IF (5.38 MHz)
3. Differential IF input with programmable input signal level : 0.5 Vpp to 2 Vpp
4. NTSC interference rejection capability
5. Compensate echo up to -5 to +47 us range
6. On-chip 10-bit ADC for HDTV demodulator
7. On-chip programmable gain amplifier

- 
8. 25MHZ crystal for clock generation
  9. Full-digital timing recovery , no VCXO is required
  10. Full-digital frequency offset recovery with wide acquisition range –1MHZ~+1MHZ
  11. Dual digital AGC control for IF and RF respectively
  12. MPEG-2 transport stream output in parallel or serial format
  13. On-chip error rate estimators for TS packets , TCM decoder , and equalizer
  14. EIA/CEA-909 antenna interface
  15. Controlled by I2C interface
  16. Supports sleep mode to save power consumption
  17. Core power supply : 1.8V , peripheral power supply : 3.3V
  18. 100-LQFP package

### **MT5351 Application :**

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux , HD MPEG-2 video decoder , JPEG decoder , MPEG1,2,MP3,AC3 audio decoder , HDTV encoder . The MT5351 enables consumer electronics manufactures to build high quality , feature-rich DTV , STB or other home entertainment audio/video device.

World-Leading Technology : HW support worldwide major broadcast network and CA standards , include ATSC , DVB , OpenCable , DirectTV , MHP.

Rich Feature for high value product : To enrich the feature of DTV , the MT5351 support 1394-5C component to external DVHS . Dual display , PIP/POP and quad pictures provide user a whole new viewing experience.

Credible Audio/Video Quality : The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback , The embedded 4X over-sample video DAC could generate very fine display quality . Also , the audio 3D surround and equalizer provide professional entertainment.

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## General Feature List :

### A . Host CPU:

1. ARM 926EJ
2. 16K I-Cache and 16K D-Cache
3. 8K Data TCM and 8K instruction
4. JTAG ICE interface
5. Watch Dog timers

### B . Transport Demuxer :

1. Support 3 independent transport stream inputs
2. Support serial/parallel interface for each transport stream input
3. Support ATSC , DVB , and MPEG2 transport stream inputs.
4. Programmable sync detection.
5. Support DES/3-DES De-scramble.
6. 96 PID filter and 128 section filters.
7. Support TS recording via IEEE1394 interface.

### C . MPEG2 Decoder :

1. Support dual MPEG-2 HD decoder or up to 8 SD decoder.
2. Complaint to [MP@ML](#) , [MP@HL](#) and MPEG-1 video standards.

### D . JPEG Decoder :

1. Decode Base-line or progressive JPEG file.

### E . 2D Graphics :

1. Support multiple color modes.
2. Point , horizontal/vertical line primitive drawing.
3. Rectangle fill and gradient fill functions.
4. Bitblt with transparent , alpha blending , alpha composition and stretch.
5. Font rendering by color expansion.
6. Support clip masks.
7. YCrCb to RGB color space transfer.

### F . OSD Display :

1. 3 linking list OSDs with multiple color mode.
2. OSD scaling with arbitrary ratio from 1/2x to 2x.
3. Square size , 32x32 or 64x64 pixel , hardware cursor.

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G . Video Processing :

1. Advanced Motion adaptive de-interlace on SDTV resolution.
2. Support clip
3. 3:2/2:2 pull down source detection.
4. Arbitrary ratio vertical/horizontal scaling of video , from 1/15X to 16X.
5. Support Edge preserve.
6. Support horizontal edge enhancement.
7. Support Quad-Picture.

H . Main Display :

1. Mixing two video and three OSD and hardware cursor.
2. Contrast/Brightness adjustment.
3. Gamma correction.
4. Picture-in-Picture( PIP ).
5. Picture-Out-Picture( POP ).
6. 480i/576i/480p/576p/720p/1080i output

I . Auxiliary Display :

1. Mixing one video and one OSD.
2. 480i/576i output.

J . TV Encoder :

1. Support NTSC M/N , PAL M/N/B/D/G/H/I
2. Macrovision Rev 7.1.L1
3. CGMS/WSS.
4. Closed Captioning.
5. Six 12-bit video DACs for CVBS , S-video or RGB/YPbPr output.

K . Digital Video Interface :

1. Support SAV/EAV.
2. Support 8/16 for SD/HD digital video input.
3. Support 8/16/24 bits digital output for main display.
4. Support 8 bits digital output for aux display.

L . DRAM Controller :

1. Support 64Mb to 1Gb DDR DRAM devices.
2. Configurable 32/64 bit data bus interface.
3. Support DDR266 , DDR333 , DDR400 , JEDEC specification compliant SDRAM.

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M . Peripheral Bus Interface :

1. Support NOR/NAND flash.
2. Support CableCard host control bus.

N . Audio :

1. Support Dolby Digital AC-3 decoding.
2. MPEG-1 layer I/II , MP3 decoding.
3. Dolby prologic II.
4. Main audio output : 5.1ch + 2ch ( down mix )
5. Auxiliary audio output : 2ch.
6. Pink noise and white noise generator.
7. Equalizer.
8. Bass management.
9. 3D surround processing include virtual surround.
10. Audio and video lip synchronization.
11. Support reverberation.
12. SPDIF out.
13. I2S I/F.

O . Peripherals :

1. Three UARTs with Tx and Rx FIFO , two of them have hardware flow control.
2. Two serial interfaces , one is master only the other can be set to master mode or slave mode.
3. Two PWMs.
4. IR blaster and receiver.
5. IEEE1394 link controller.
6. IDE bus : ATA/ATAPI7 UDMA mode 5 , 100MB/s.
7. Real-time clock and watchdog controller.
8. Memory card I/F : MS/MS-pro ,SD ,CF ,and MMC
9. PCMCIA/POD/CI interface

P . IC Outline :

1. 471 Pin BGA Package.
2. 3.3V/1.2V dual Voltage.

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## **MX29LV320BTTC (Flash) Application :**

The MX29LV320AT/B is a 32-mega bit Flash memory organized as 4M bytes of 8 bits and 2M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory.

The MX29LV320AT/B is packaged in 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers. The standard MX29LV320AT/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV320AT/B has separate chip enable (CE) and output enable (OE) controls.

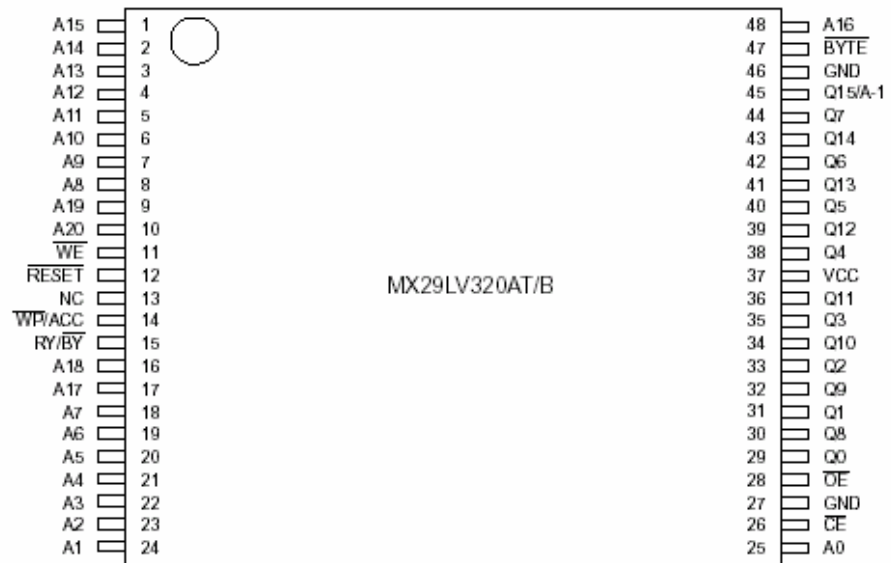
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV320AT/B uses a command register to manage this functionality. MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling.

The MX29LV320AT/B uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

## PIN CONFIGURATION

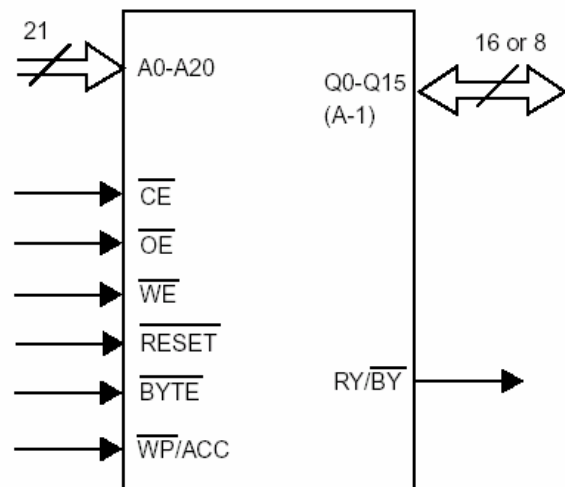
### 48 TSOP



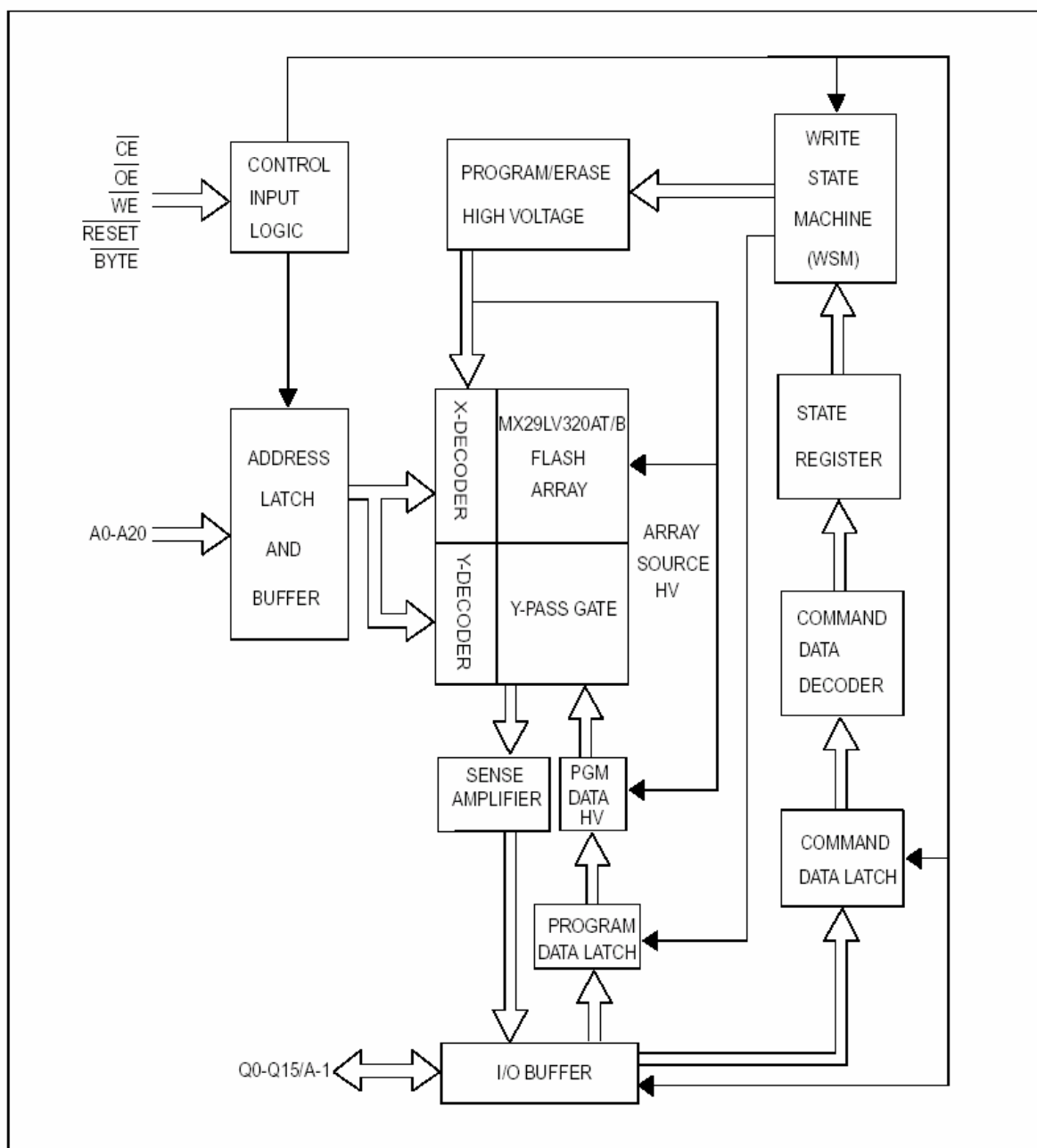
### PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	15 Data Inputs/Outputs
Q15/A-1	Q15(Data Input/Output, word mode) A-1(LSB Address Input, byte mode)
CE	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
BYTE	Word/Byte Selection Input
RESET	Hardware Reset Pin, Active Low
RY/BY	Read/Busy Output
VCC	3.0 volt-only single power supply
WP/ACC	Hardware Write Protect/Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally

### LOGIC SYMBOL



## BLOCK DIAGRAM



## BUS OPERATION--1

Operation	CE	OE	WE	RESET	WP/ACC	Addresses (Note 2)	Q0~Q7	Q8 ~ Q15	
								Byte=VIH	Byte=VIL
Read	L	L	H	H	L/H	A <sub>IN</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	Q8-A14 =High-Z Q15=A-1
Write (Note 1)	L	H	L	H	Note 3	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	
Accelerate Program	L	H	L	H	V <sub>HH</sub>	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	
Standby	VCC ± 0.3V	X	X	VCC ± 0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V <sub>ID</sub>	L/H	Sector Addresses, A6=L, A1=H, A0=L	D <sub>IN</sub> , D <sub>OUT</sub>	X	X
Chip Unprotect (Note 2)	L	H	L	V <sub>ID</sub>	Note 3	Sector Addresses, A6=H, A1=H, A0=L	D <sub>IN</sub> , D <sub>OUT</sub>	X	X
Temporary Sector Group Unprotect	X	X	X	V <sub>ID</sub>	Note 3	A <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	High-Z

### Legend:

L=Logic LOW=VIL, H=Logic High=VIH, VID=12.0 0.5V, VHH=11.5-12.5V, X=Don't Care,  
AIN=Address IN, DIN=Data IN,DOUT=Data OUT

### Notes:

1. When the WP/ACC pin is at VHH, the device enters the accelerated program mode. See "Accelerated Program Operations" for more information.
- 2.The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotection" section.
- 3.If WP/ACC=VIL, the two outermost boot sectors remain protected. If WP/ACC=VIH, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP/ACC=VHH, all sectors will be unprotected.
- 4.DIN or Dout as required by command sequence, data polling, or sector protection algorithm.
- 5.Address are A20:A0 in word mode (BYTE=VIH), A20:A-1 in byte mode (BYTE=VIL).

## BUS OPERATION--2

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0-Q7	Q8-Q15
Read Silicon ID Manufacturer Code	L	L	H	X	X	$V_{ID}$	X	L	X	L	L	C2H	X
Read Silicon ID MX29LV320AT	L	L	H	X	X	$V_{ID}$	X	L	X	L	H	A7H	22h(word) X (byte)
Read Silicon ID MX29LV320AB	L	L	H	X	X	$V_{ID}$	X	L	X	L	H	A8H	22h(word) X (byte)
Sector Protect Verification	L	L	H	SA	X	$V_{ID}$	X	L	X	H	L	01h(1), or 00h	X
Security Sector Indicator Bit (Q7)	L	L	H	X	X	$V_{ID}$	X	L	X	H	H	99h(2), or 19h	X

Notes:

- 1.Code=00h means unprotected, or code=01h protected.
- 2.Code=99 means factory locked, or code=19h not factory locked.

## WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive WE and CE to VIL, and OE to VIH.

An erase operation can erase one sector, multiple sectors , or the entire device. A "sector address" consists of the address bits required to uniquely select a sector. Writing specific address and data commands or sequences into the command register initiates device operations. Table A defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation. After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

**TABLE A. MX29LV320AT/B COMMAND DEFINITIONS**

Command	Bus Cycles	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read(Note 5)	1	RA	RD										
Reset(Note 4)	1	XXX	F0										
Automatic Select(Note 5)													
Manufacturer ID	Word	4	555 AA	2AA 55	555 90	X00	C2H						
	Byte	4	AAA AA	555 55	AAA 90	X00	C2H						
Device ID	Word	4	555 AA	2AA 55	555 90	X01	ID						
	Byte	4	AAA AA	555 55	AAA 90	X02							
Security Sector Factory	Word	4	555 AA	2AA 55	555 90	X03	99/19						
Protect Verify (Note 6)	Byte	4	AAA AA	555 55	AAA 90	X06							
Sector Protect Verify (Note 7)	Word	4	555 AA	2AA 55	555 90	(SA)X02	00/01						
	Byte	4	AAA AA	555 55	AAA 90	(SA)X04							
Enter Security Sector Region	Word	3	555 AA	2AA 55	555 88								
	Byte	3	AAA AA	555 55	AAA 88								
Exit Security Sector	Word	4	555 AA	2AA 55	555 90	XXX 00							
	Byte	4	AAA AA	555 55	AAA 90	XXX 00							
Program	Word	4	555 AA	2AA 55	555 A0	PA	PD						
	Byte	4	AAA AA	555 55	AAA A0	PA	PD						
Chip Erase	Word	6	555 AA	2AA 55	555 80	555 AA	2AA 55	555 55	555 10				
	Byte	6	AAA AA	555 55	AAA 80	AAA AA	555 55	AAA 10					
Sector Erase	Word	6	555 AA	2AA 55	555 80	555 AA	2AA 55	555 SA	30				
	Byte	6	AAA AA	555 55	AAA 80	AAA AA	555 55	SA 30					
CFI Query (Note 8)	Word	1	55 98										
	Byte	1	AA 98										
Erase Suspend(Note 9)	1	SA	B0										
Erase Resume(Note 10)	1	SA	30										

**Legend:**

X=Don't care

RA=Address of the memory location to be read.

RD=Data read from location RA during read operation.

PA=Address of the memory location to be programmed.

Addresses are latched on the falling edge of the WE or CE pulse.

PD=Data to be programmed at location PA. Data is latched on the rising edge of WE or CE pulse.

SA=Address of the sector to be erased or verified. Address bits A20-A12 uniquely select any sector.

ID=22A7h(Top), 22A8h(Bottom)

**Notes:**

- 1.All values are in hexadecimal.
- 2.Except when reading array or Automatic Select data, all bus cycles are write operation.
- 3.The Reset command is required to return to the read mode when the device is in the Automatic Select mode or if Q5 goes high.
- 4.The fourth cycle of the Automatic Select command sequence is a read cycle.
- 5.The data is 99h for factory locked and 19h for not factory locked.
- 6.The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block. In the third cycle of the command sequence, address bit A20=0 to verify sectors 0~31, A20=1 to verify sectors 32~70 for Top Boot device.
- 7.Command is valid when device is ready to read array data or when device is in Automatic Select mode.
- 8.The system may read and program functions in non-erasing sectors, or enter the Automatic Select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
- 9.The Erase Resume command is valid only during the Erase Suspend mode.

---

## STANDBY MODE

MX29LV320AT/B can be set into Standby mode with two different approaches. One is using both CE and RESET pins and the other one is using RESET pin only.

When using both pins of CE and RESET, a CMOS Standby mode is achieved with both pins held at  $V_{cc} \pm 0.3V$ . Under this condition, the current consumed is less than 0.2uA (typ.). If both of the CE and RESET are held at  $V_{IH}$ , but not within the range of  $V_{CC} \pm 0.3V$ , the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation,  $V_{cc}$  active current ( $ICC2$ ) is required even CE = "H" until the operation is completed. The device can be read with standard access time ( $t_{CE}$ ) from either of these standby modes.

When using only RESET, a CMOS standby mode is achieved with RESET input held at  $V_{ss} \pm 0.3V$ . Under this condition the current is consumed less than 1uA (typ.). Once the RESET pin is taken high, the device is back to active without recovery delay.

In the standby mode the outputs are in the high impedance state, independent of the OE input.

MX29LV320AT/B is capable to provide the Automatic Standby Mode to restrain power consumption during readout of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX29LV320AT/B automatically switch themselves to low power mode when MX29LV320AT/B addresses remain stable during access time of  $t_{ACC}+30ns$ . It is not necessary to control CE, WE, and OE on the mode. Under the mode, the current consumed is typically 0.2uA (CMOS level).

## RESET OPERATION

01The RESET pin provides a hardware method of resetting the device to reading array data. When the RESET pin is driven low for at least a period of  $t_{RP}$ , the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET pulse. When RESET is held at  $V_{SS} \pm 0.3V$ , the device draws CMOS standby current ( $ICC4$ ). If RESET is held at  $V_{IL}$  but not within  $V_{SS} \pm 0.3V$ , the standby current will be greater.

The RESET pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firm-ware from the Flash memory.

If RESET is asserted during a program or erase operation, the RY/BY pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of  $t_{READY}$  (during Embedded Algorithms).

---

The system can thus monitor RY/BY to determine whether the reset operation is complete. If RESET is asserted when a program or erase operation is not executing (RY/BY pin is "1"), the reset operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET pin returns to VIH. Refer to the AC Characteristics tables for RESET parameters and to Figure 14 for the timing diagram.

### **WRITE PROTECT (WP)**

The write protect function provides a hardware method to protect boot sectors without using VID. If the system asserts VIL on the WP/ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in Sector/Sector Group Protection and Chip Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts VIH on the WP/ACC pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Group Protection and Chip Unprotection".

Note that the WP/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

### **SOFTWARE COMMAND DEFINITIONS :**

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (when applicable).

All addresses are latched on the falling edge of WE or CE, whichever happens later. All data are latched on rising edge of WE or CE, whichever happens first.

### **WRITE OPERATION STATUS**

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY. Table B and the following subsections describe the functions of these bits. Q7, RY/BY, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

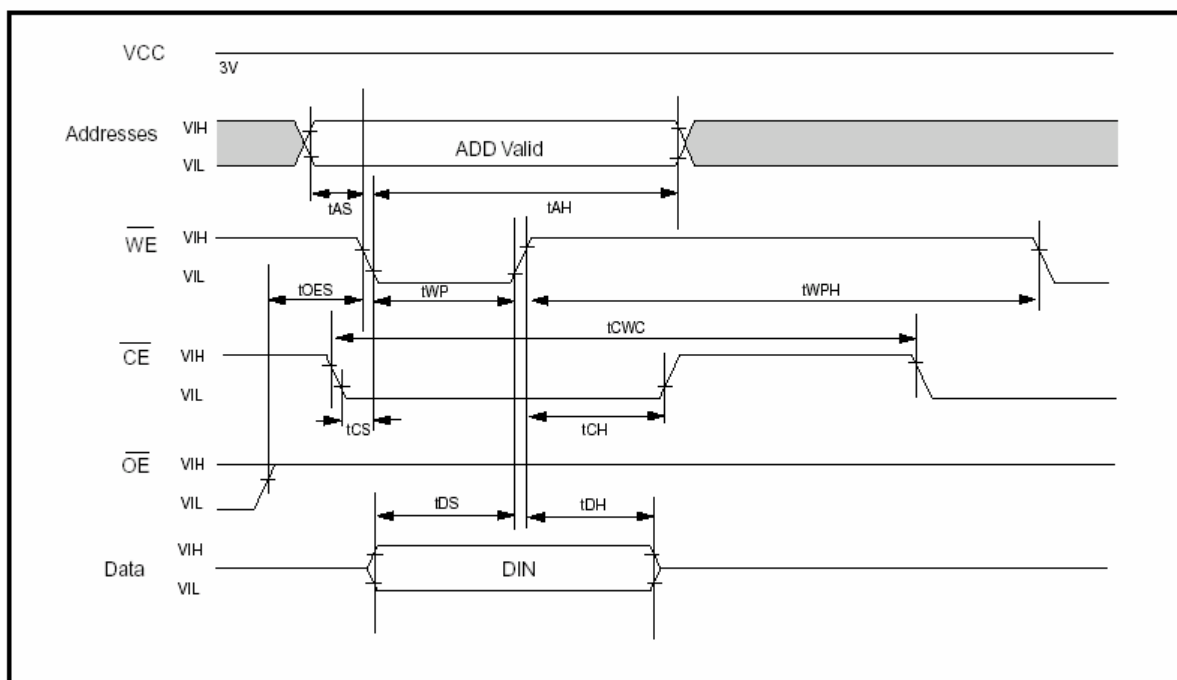
**Table B. Write Operation Status**

In Progress	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2	RY/BY
	Byte/Word Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A	0
	Exceeded Time Limits	Byte/Word Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
		Auto Erase Algorithm	0	Toggle	1	1	Toggle	0
Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A	0	

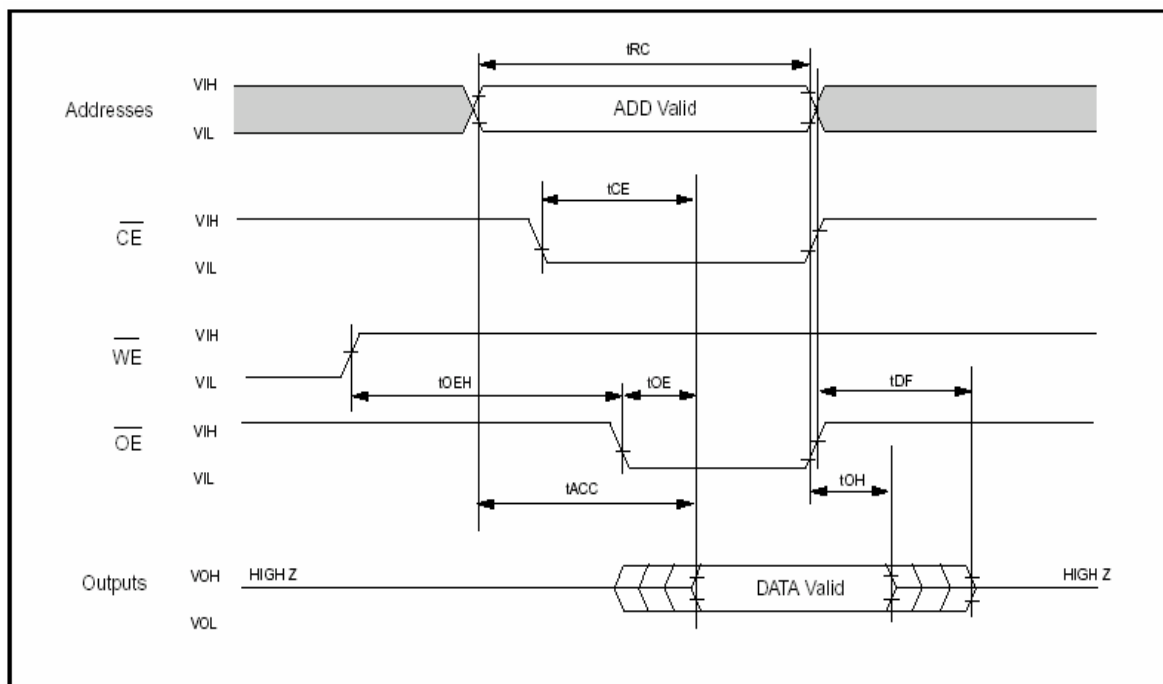
**Notes:**

- 1.Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
- 2.Performing successive read operations from any address will cause Q6 to toggle.
- 3.Reading the byte/word address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit.  
However, successive reads from the erase-suspended sector will cause Q2 to toggle.

**Fig C. COMMAND WRITE OPERATION**



**Fig D. READ TIMING WAVEFORMS**

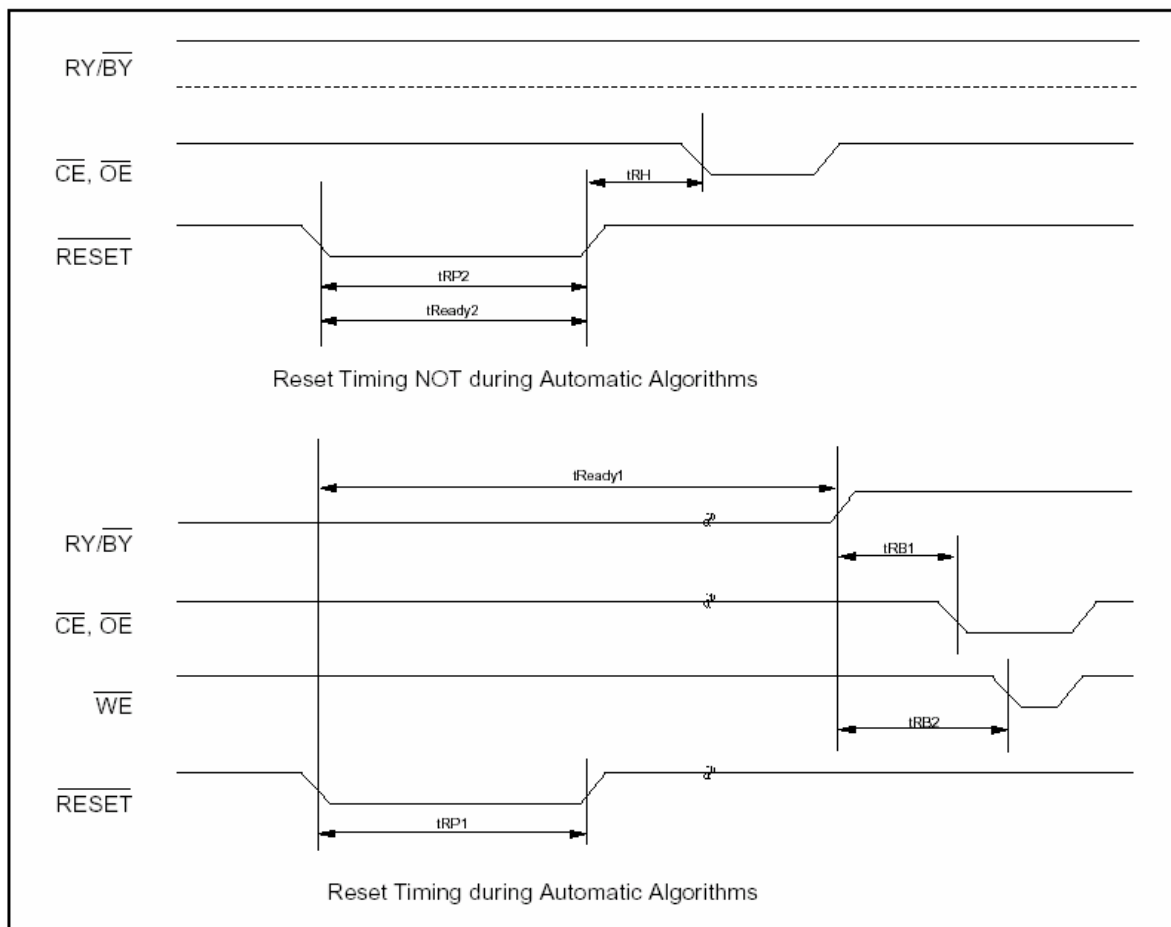


#### AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	RESET Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	RESET Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET High Time Before Read(See Note)	MIN	70	ns
tRB1	RY/BY Recovery Time(to $\overline{CE}$ , $\overline{OE}$ go low)	MIN	0	ns
tRB2	RY/BY Recovery Time(to $\overline{WE}$ go low)	MIN	50	ns

Note:Not 100% tested

**Fig E. RESET TIMING WAVEFORM**



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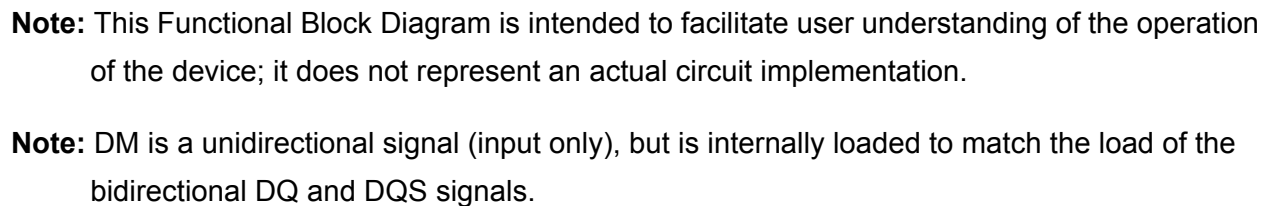
## **DDR SDRAM (NT5DS16M16CS-5T) Application : Functional Description**

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268, 435, 456 bits. The 256Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a  $2n$  prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM consists of a single  $2n$ -bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit wide, one-half clock cycle data transfers at the I/O pins.

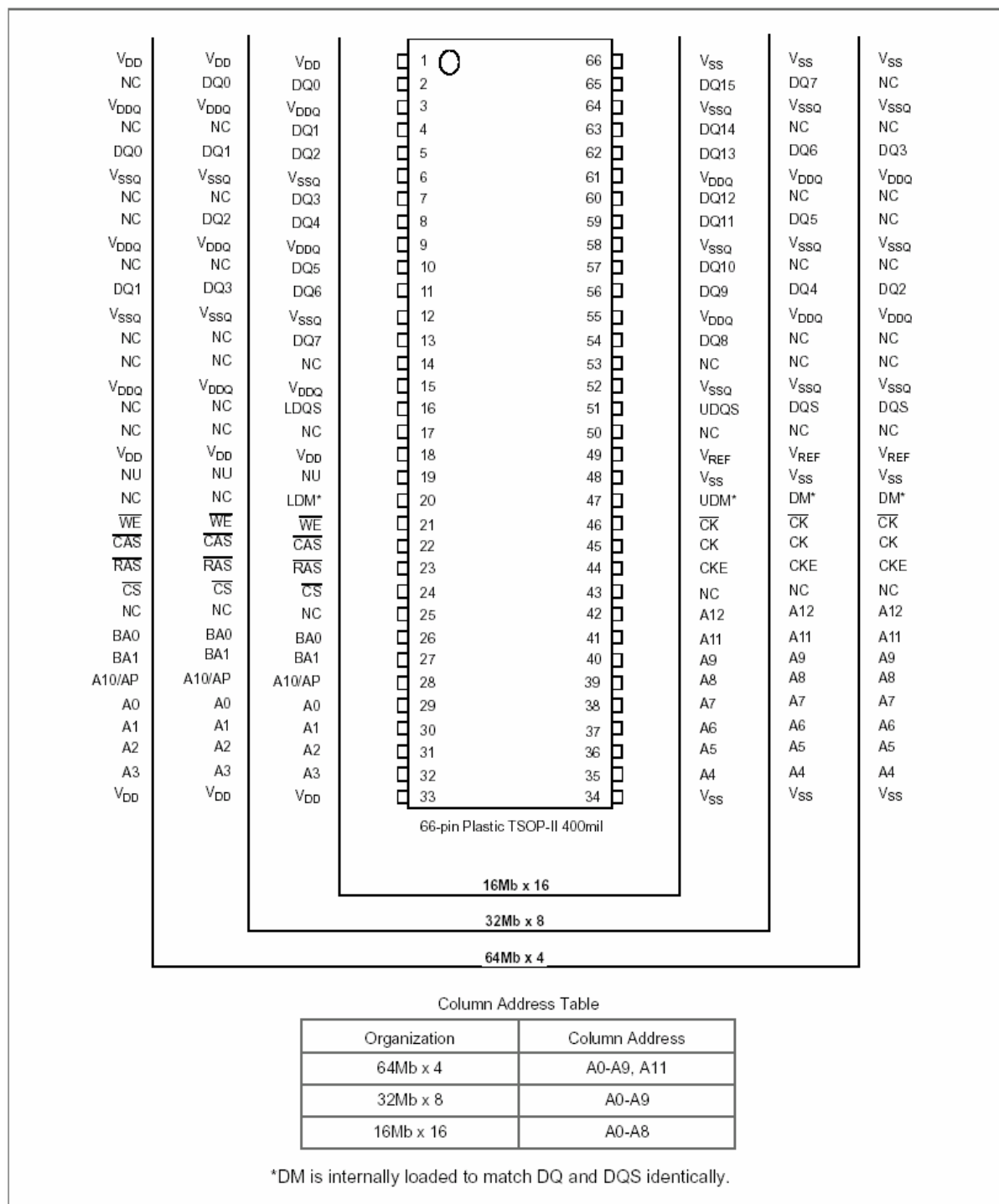
Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

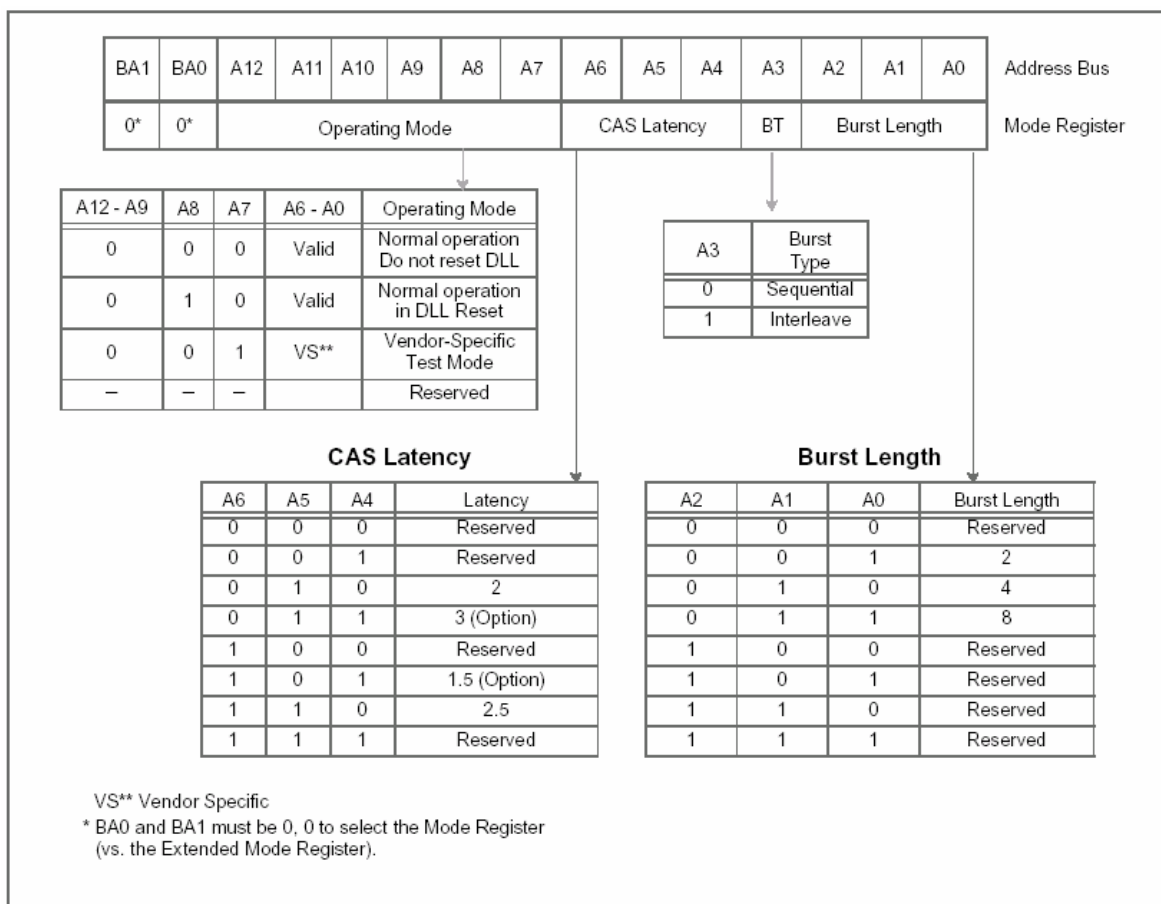


**Note:** DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

## Pin Configuration - 400mil TSOP II (x4 / x8 / x16)



## Mode Register Operation



## Operating Mode

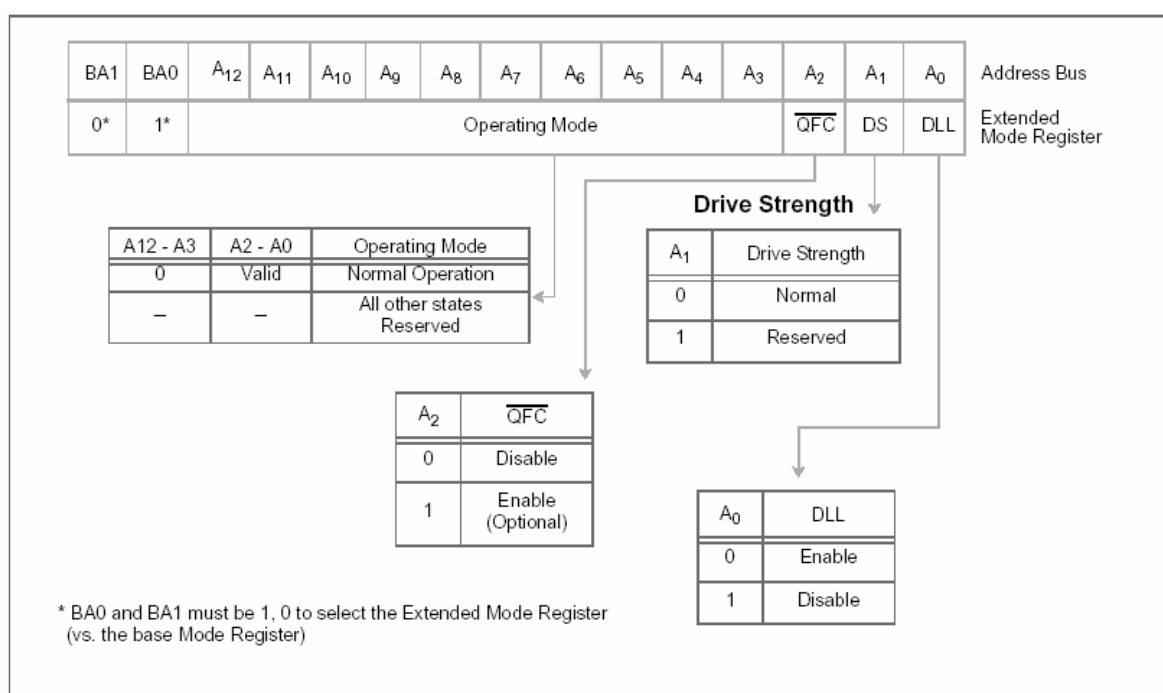
The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

## Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, bit A0; output drive strength selection, bit A1; and QFC output enable/disable, bit A2 (NTC optional). These functions are controlled via the bit settings shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

## Extended Mode Register Definition



## Truth Table a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (Nop)	H	X	X	X	X	NOP	1, 9
No Operation (Nop)	L	H	H	H	X	NOP	1, 9
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1, 3
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1, 4
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1, 4
Burst Terminate	L	H	H	L	X	BST	1, 8
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1, 5
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR / SR	1, 6, 7
Mode Register Set	L	L	L	L	Op-Code	MRS	1, 2

1. CKE is high for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects ,Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0, BA1 provide bank address; A0-Ai provide column address (where  $i = 9$  for x8 and 9, 11 for x4); A10 high enables the Auto Precharge feature (non-persistent), A10 low disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged.A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care."
6. This command is auto refresh if CKE is high; Self Refresh if CKE is low.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts
9. Deselect and NOP are functionally interchangeable.

### Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0,BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

### Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where  $[i = 9, j = \text{don't care}]$  for x8; where  $[i = 9, j = 11]$  for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

---

## **Write**

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

## **Auto Refresh**

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to CAS Before RAS (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The 256Mb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8  $\mu$ s (maximum).

## **Self Refresh**

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are "Don't Care" during Self Refresh operation.

The procedure for exiting self refresh requires a sequence of commands. CK (and CK) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

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## Operations :

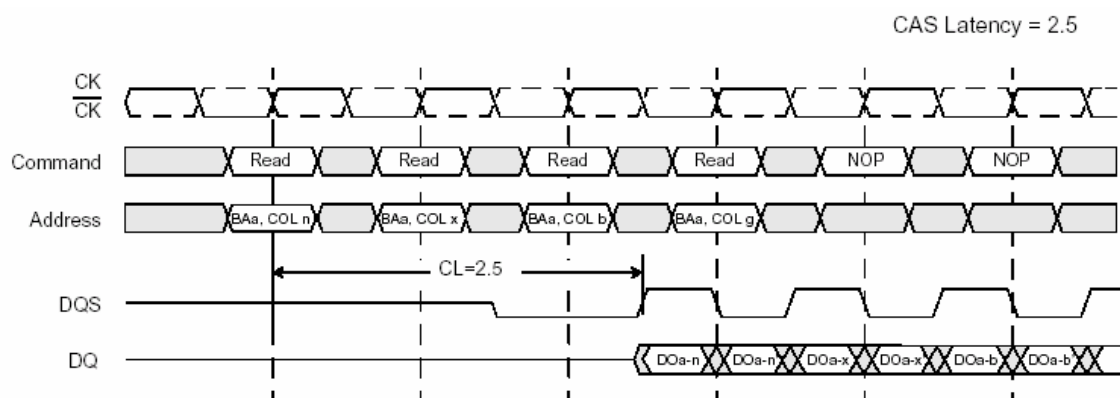
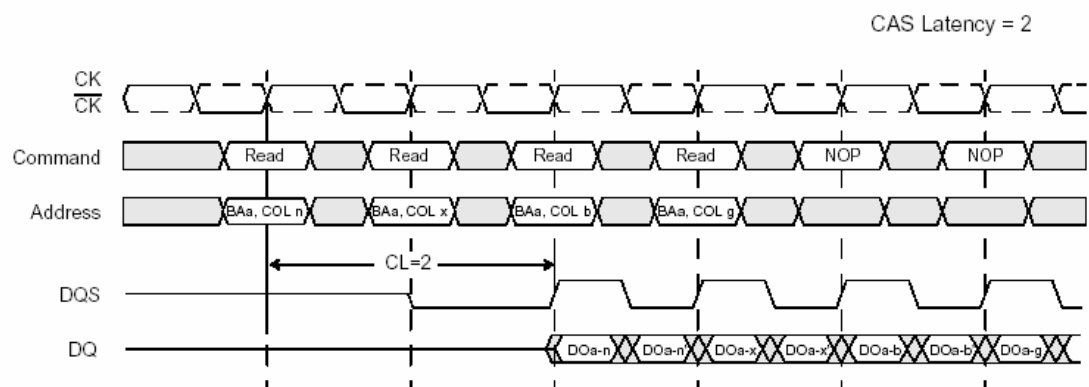
### Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command.


The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided tRAS has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and CK). The following timing figure entitled "Read Burst: CAS Latencies (Burst Length=4)" illustrates the general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure entitled "Consecutive Read Bursts: CAS Latencies (Burst Length =4 or 8)". A Read command can be initiated on any positive clock cycle following a previous Read command. Nonconsecutive Read data is shown in timing figure entitled "Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)". Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed as shown on following:

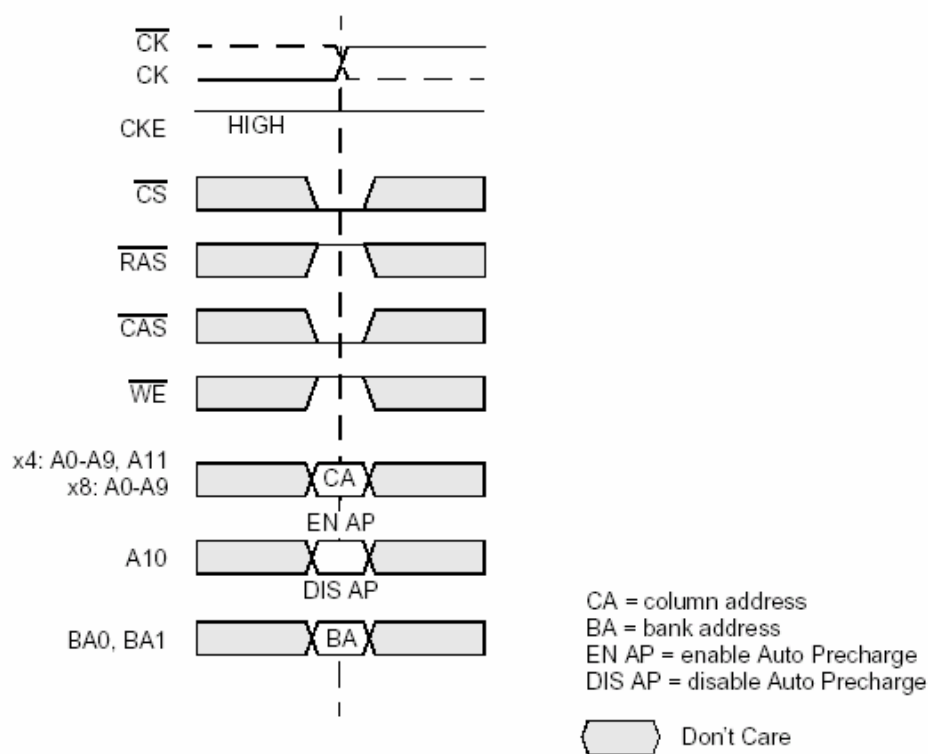
## Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)



DO a-n, etc. = data out from bank a, column n etc.  
 n' etc. = odd or even complement of n, etc. (i.e., column address LSB inverted).  
 Reads are to active rows in any banks.  
 Shown with nominal  $t_{AC}$ ,  $t_{DQSQ}$ , and  $t_{DQSQ}$ .

 Don't Care

## Read Command



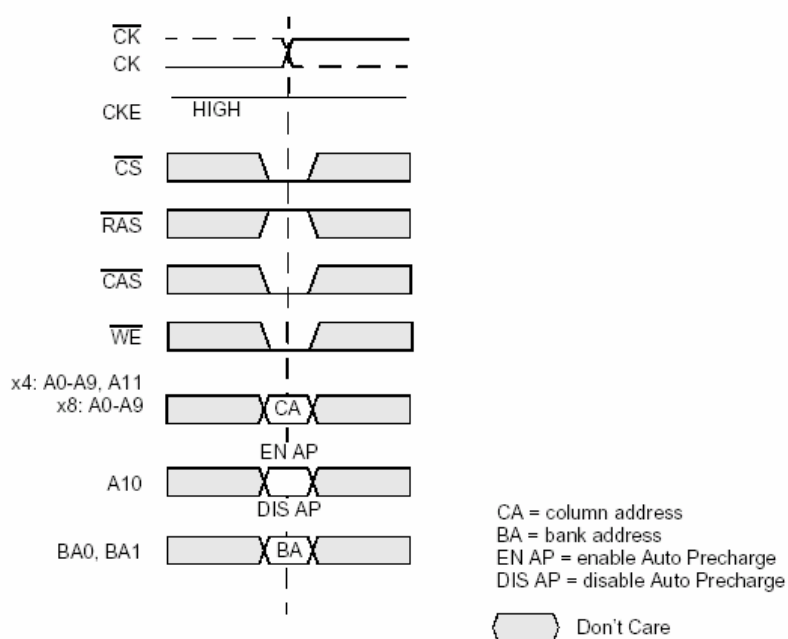
## Writes

Write bursts are initiated with a Write command, as shown in timing figure *Write Command* on following: The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

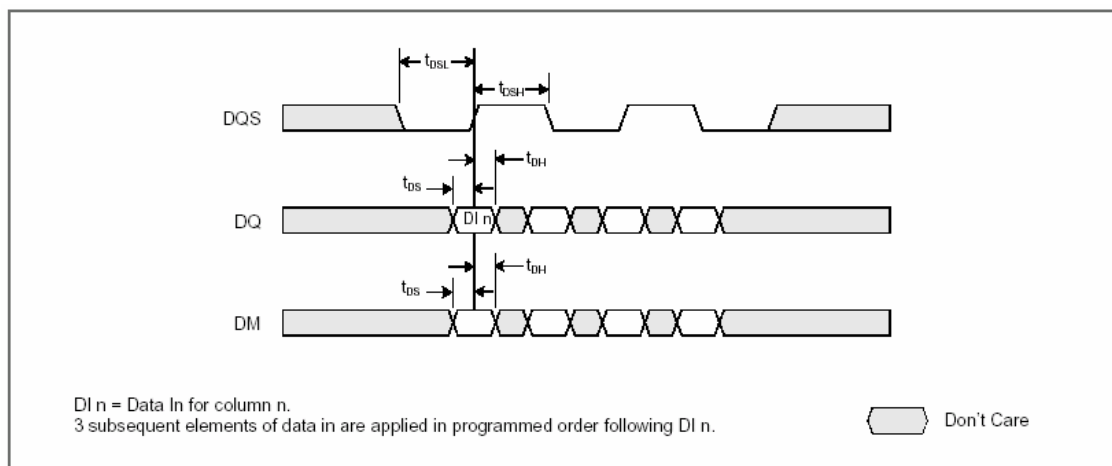
During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. tDQSS(min) and tDQSS(max)). Timing figure *Write Burst (Burst Length = 4)* on page 33 shows the two extremes of tDQSS for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture).

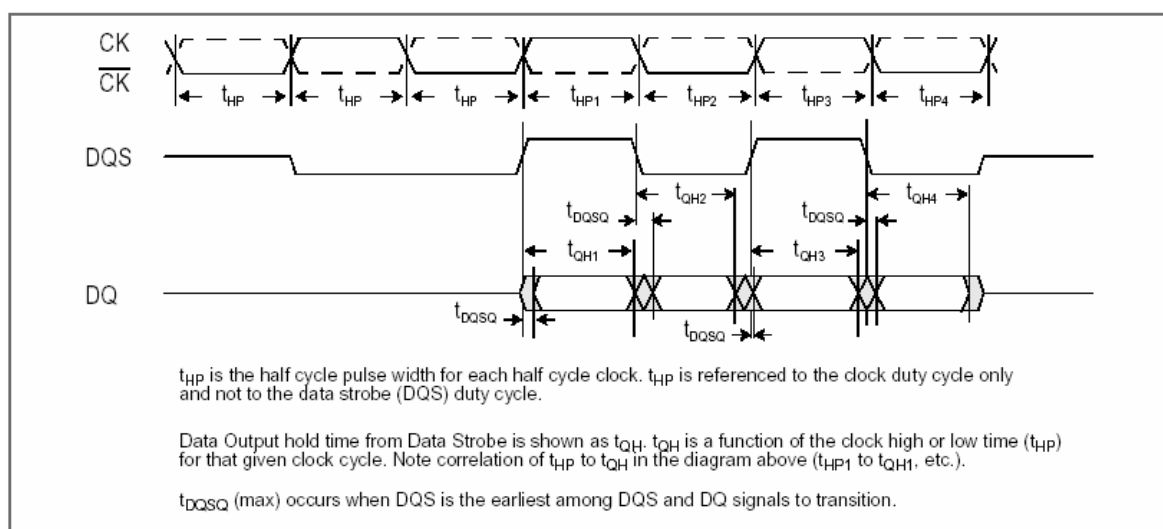
## Write Command



## Data Input (Write)



## Data Output (Read)

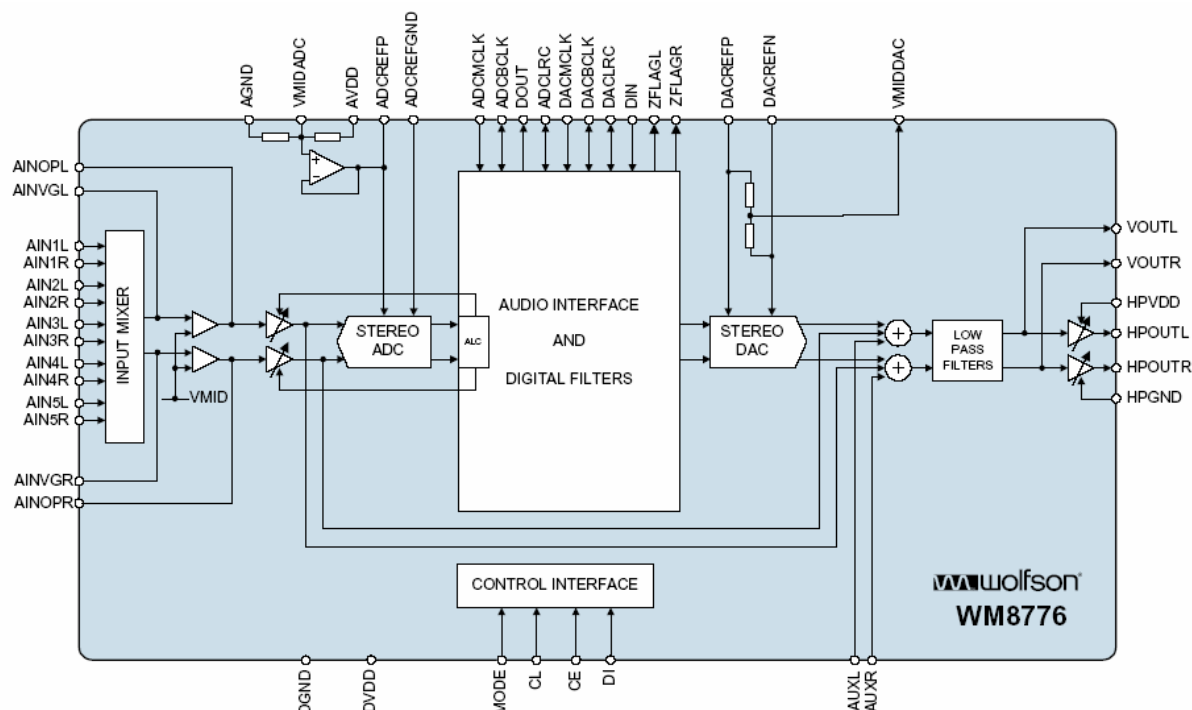


## WM8776 Application

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audiovisual equipment. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with control for the headphone

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I2S, left justified, right justified and DSP formats.

## BLOCK DIAGRAM



### 1. Audio sample rate

The master clock for WM8776 supports DAC and ADC audio sampling rates 256fs to 768fs, where fs is the audio sample frequency (DACLRC or ADCLRC) typically 32KHZ, 44.1KHZ, 48KHZ or 96KHZ (the DAC also supports operation at 128fs and 192fs and 192KHZ sample rate). The master clock is used to operate the digital filters and the noise shaping circuits.

In slave mode the WM8776 has a master detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks) If there is a greater than 32 clocks error the interface is disabled and ADCLRC/DACLRC for optimal performance, although the WM8776 is tolerant of phase variations or jitter on this clock.

Table shows the typical master clock frequency inputs for the WM8776.

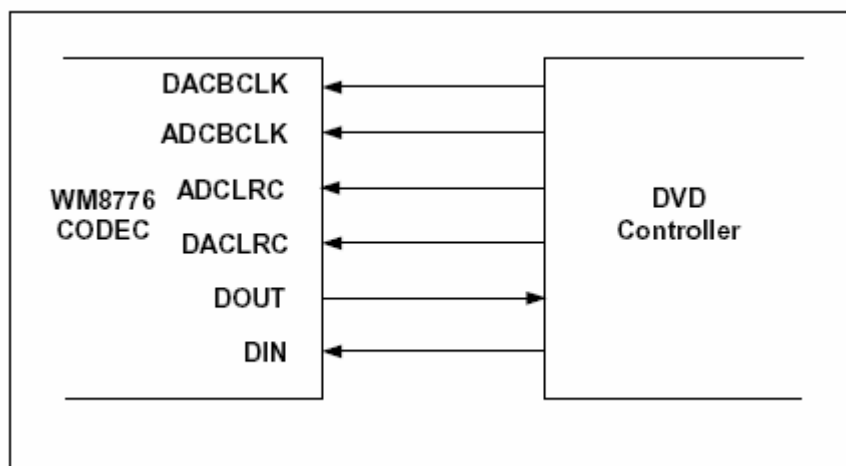
SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	DAC ONLY					
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

## 2. DIGITAL AUDIO INTERFACE

### a. Slave mode

The audio interfaces operations in either slave mode selectable using the MS control bit. In slave mode DIN is always an input to the WM8776 and DOUT is always an output. The default is Slave mode. In slave mode (ms=0) ADCLRC, DACLRC, ADCBCLK, DACBCLK are input to the WM8776 .

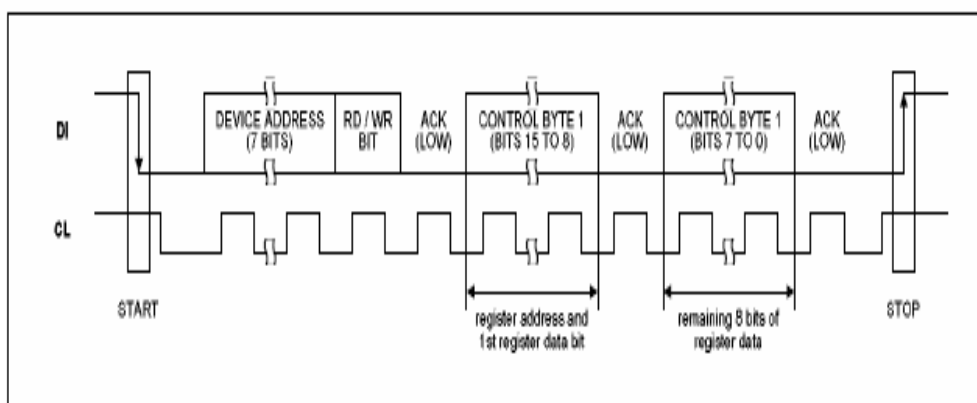
DIN and DACLRC are sampled by the WM8776 on the rising edge of DACBCLK; ADCLRC is sampled on the rising edge of ADCBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK. By setting control bit BCLKINV the polarity of ADCBCLK and DACBCLK may be reversed so that DIN and DACLRC are sample on the falling edge of DACBCLK, ADCLRC is sampled on the falling edge of ADCBCLK and DOUT changes on the rising of ADCBCLK Slave mode as shown in the following figure.



## b. 2 Wire serial control mode

The wm8776 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the wm8776). The wm8776 operates as a slave device only.

2-wire serial interface as shown in the following figure.



The wm8776 has two possible device addresses, which can be selected using the CE pin. In the L37 LCD TV, the CE pin is LOW (device address is 34h).

CE STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

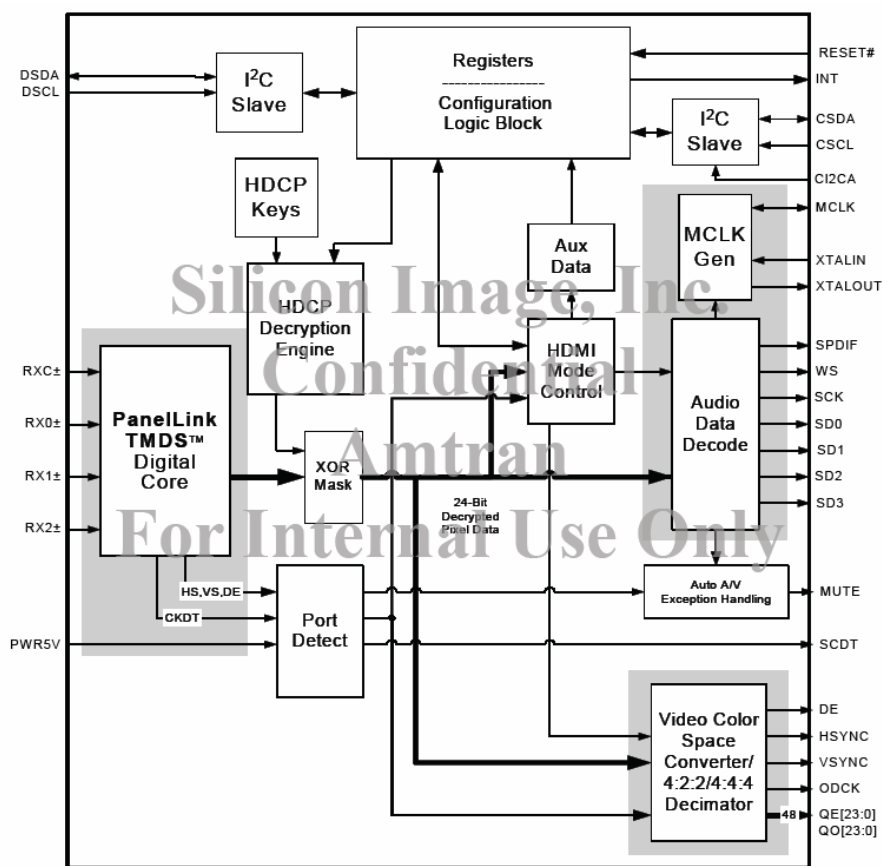
In the L37, the wm8776 has a 2-wire interface.

MODE	Control Mode
0	2 wire interface
1	3 wire interface

## Sil9011 Application

The sil9011 provides a complete solution for receiving HDMI compliant digital audio and video. Specialized audio and video processing is available within the sil9011 to easily and cost effectively adds HDMI capability to consumer electronics devices such as digital TVs, plasma displays, LCD TVs and projectors.

## BLOCK DIAGRAM



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## 1. TMDS Digital Core

The core performs 10-to-8-bit TMDS decoding on the audio and video received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core supports link clock rates to 165MHz, including CE modes to 720P/1080I/1080P.

## 2. Active port detection

The Pane Link core detects an active TMDS clock and actively toggling DE signal. These states are accessible in register bits, useful for monitoring the status of the HDMI input or for automatically powering down the receiver. The 5V supply from the HDMI connector is used as a cable detect indicator. The sil9011 can monitor the presence of this +5V supply and, if and when necessary, provide a fast audio mute without pops when it senses the HDMI cable pulled. The microcontroller can also poll registers in the sil9011 to check whether an HDMI cable is connected.

## 3. HDCP Decryption engine

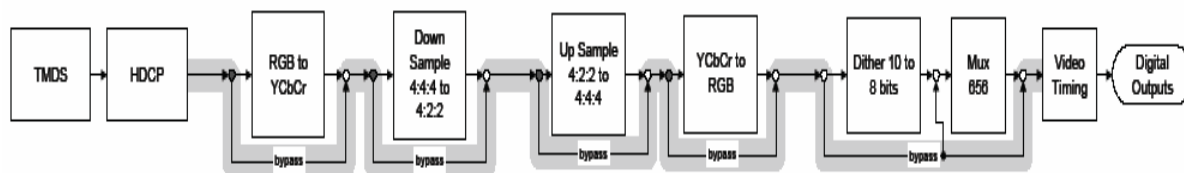
The HDCP decryption engine contains all necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host microprocessor through a set sequence of register reads and wires through the DDC channel. Pre-programmed HDCP keys and key Selection Vector are used in the decryption process. A resulting calculated to an XOR mask during each clock cycle to decrypt the audio/video data in sync with the host.

## 4. Video Data Conversion and Video Output

The Sil9011 can output video in many different formats as shown in the following figure.

Color Space	Video Format	Bus Width	HSYNC / VSYNC	Output Clock (MHz) <sup>3</sup>							Notes
				480i	480p	XGA	720p	1080i	1080p	UXGA	
RGB	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	
YCbCr	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	
YCbCr	4:2:2	16/20/24	Sep, Emb.	13.25 / 27	27	—	74.25	74.25	148.5	162	1,2
YCbCr	4:2:2	8/10/12	Sep, Emb.	27	54	135	148.5	148.5	—	—	1,4
RGB	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
YCbCr	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
RGB	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:2:2	8/10/12	Sep, Emb.	13.25/27	27	65	74.25	74.25	—	81	1,4

The receiver can also process the video data before it is output as show below figure



## 5. I<sup>2</sup>c Interface to Display Controller

The Controller I<sup>2</sup>c interface (CSDA, CSCL) on the sil9011 is a slave interface capable of running up to 400KHZ. This bus is used to configure the SIL9011 by reading/writing to the appropriate registers. The SIL9011 is accessible on the local I<sup>2</sup>c bits at two-device address. The logic state of the CI2CA pin is latched on the rising edge of REST# providing a choice of two pairs of device address.

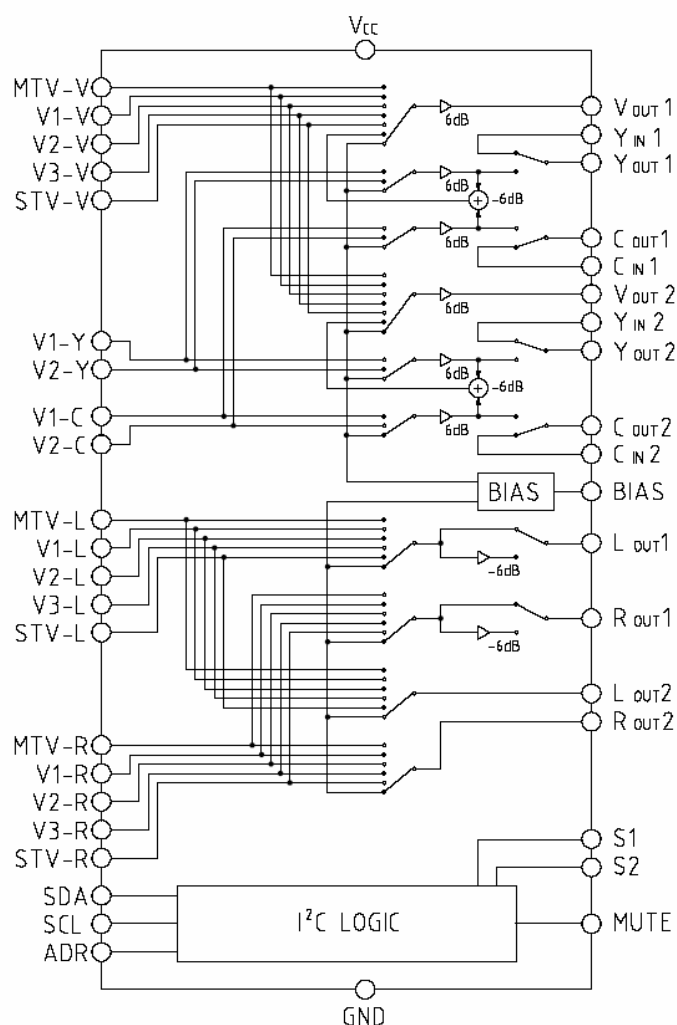
Control of local I<sup>2</sup>c address with CI2CA pin

	CI2CA = Pull Down	CI2CA = Pull Up
First Device Addr	0x60	0x62
Second Device Addr	0x68	0x6A

## MM1942 Application

The MM1942 IC is a 5-input 2-output AV switch controlled by the I<sup>2</sup>C BUS developed for use in television.

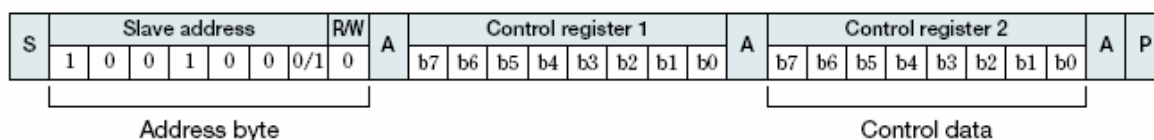
## BLOCK DIAGRAM



### 1. I<sup>2</sup>c Bus

I<sup>2</sup>C BUS is an interconnecting bus system controlled by 2 lines (SDA, SCL). Data are transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start conditions.

The data format is set as shown in the following figure.



In the L32 TV MM1492 slave address, ADDR terminal is L, and 90H is selected.

The following figure indicates the control contents of control registers and switches.

Register	b7	b6	b5	b4	b3	b2	b1	b0
1	Audio Gain 1	S/Comp select 1	Video out1 select			Audio out1 select		
2	Audio Gain 2	S/Comp select 2	Video out2 select			Audio out2 select		

## 2. Switch control table

### a. Video output 1

b6	b5	b4	b3	Vour1	Your1	Cour1
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV-V	Yin1	Cin1
0	0	1	0	V1-V	Yin1	Cin1
0	0	1	1	V2-V	Yin1	Cin1
0	1	0	0	V3-V	Yin1	Cin1
0	1	0	1	STV-V	Yin1	Cin1
0	1	1	0	Mute	Mute	Mute
0	1	1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV-V	Yin1	Cin1
1	0	1	0	V1-(Y+C)	V1-Y	V1-C
1	0	1	1	V2-(Y+C)	V2-Y	V2-C
1	1	0	0	V3-V	Yin1	Cin1
1	1	0	1	STV-V	Yin1	Cin1
1	1	1	0	Mute	Mute	Mute
1	1	1	1			

### b. Audio output 1

Mute terminal	b2	b1	b0	Lour1	Rour1
≤1.5V (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
	1	1	1		
≥3.0V				Mute	Mute

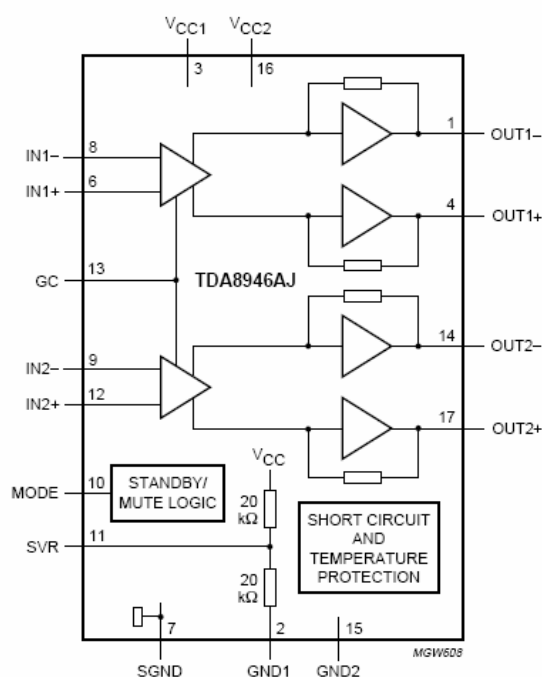
### c. Audio gain

b7	Lour1	Rour1
0	-6dB	-6dB
1	0dB	0dB

## TDA8946 Application

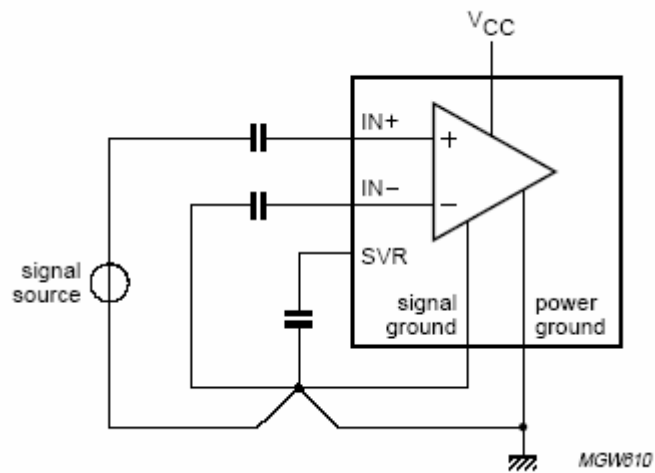
In L32 TV the TDA8946AJ is a dual-channel audio power amplifier with DC gain control. It has an output power of 2 . 10 W at an 8 . load and a 12 V supply.

### Block diagram



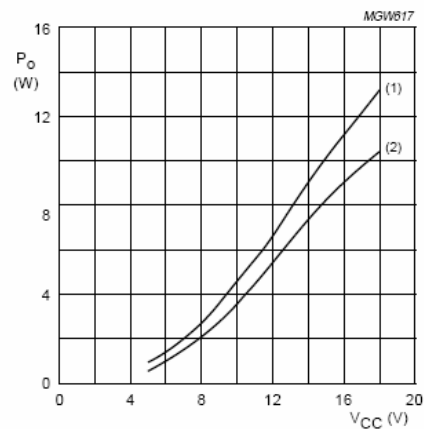
### 1. Input configuration

The TDA8946AJ inputs can be driven symmetrical (floating) as well as asymmetrical. In the asymmetrical mode one input pin is connected via a capacitor to the signal source and the other input is connected to the signal ground. The signal ground should be as close as possible to the SVR (electrolytic) capacitor ground. Note that the DC level of the input pins is half of the supply voltage VCC, so coupling capacitors for both pins are necessary.



## 2. Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10%, in the L32 LCD TV  $V_{CC}=12V$  so we can see as shown in the following figure output about 7W.



$R_L = 8 \Omega$

(1) THD = 10%

(2) THD = 1%

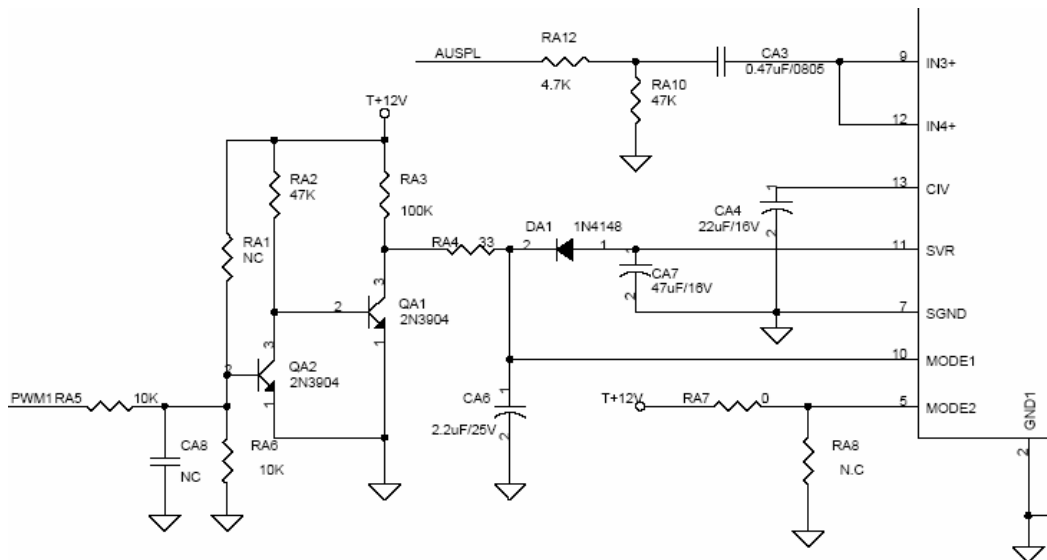
### 3. Mode selection

In the L32 LCD TV TDA8946AJ has two functional modes, which can be selected by applying the proper DC voltage to pin MODE.

**a. Mute** — In this mode the amplifier is DC-biased but not operational (no audio output).

This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when  $3.5\text{ V} < \text{VMODE} < (\text{VCC} - 1.5\text{ V})$ .

**b. Operating** — In this mode the amplifier is operating normally. The operating mode is activated at  $\text{VMODE} < 1.0\text{V}$ .

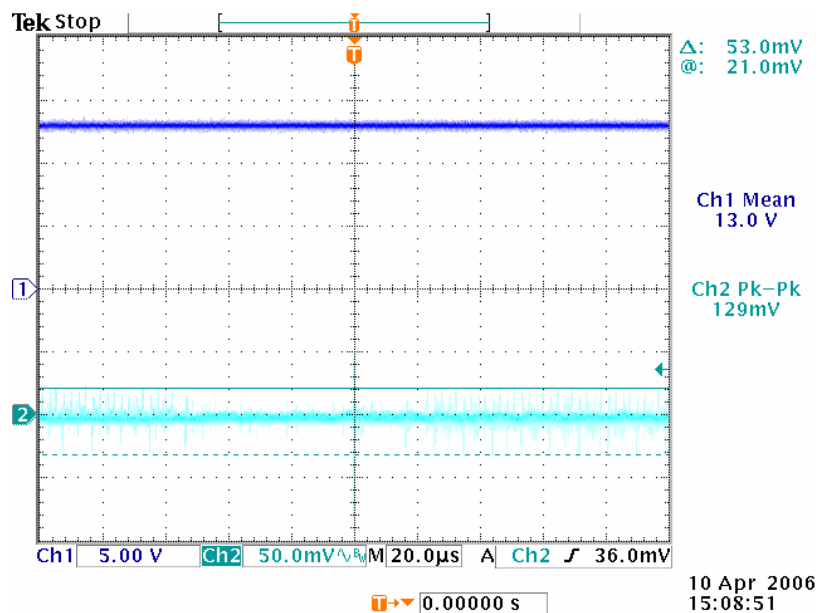


# Chapter 9 Waveforms

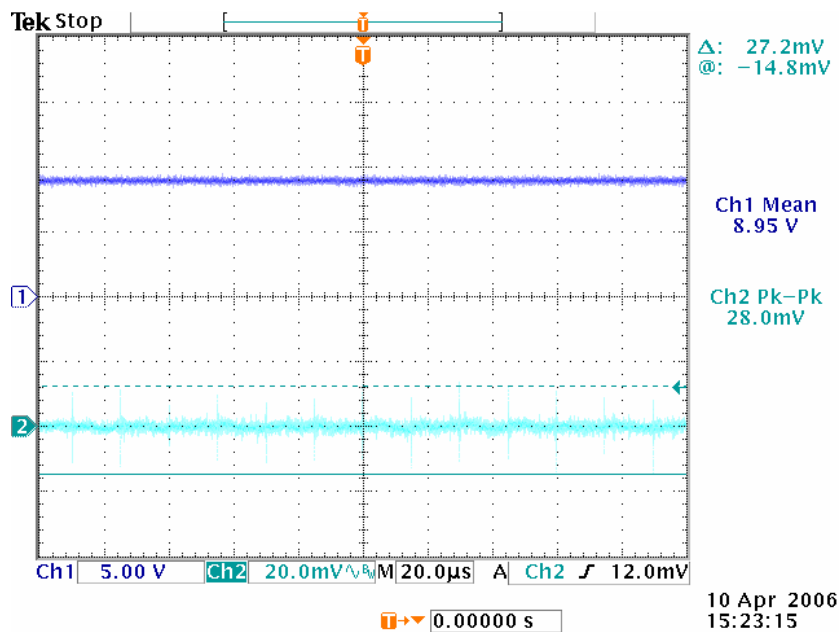
## Main Board

### 1. Voltage Measurement

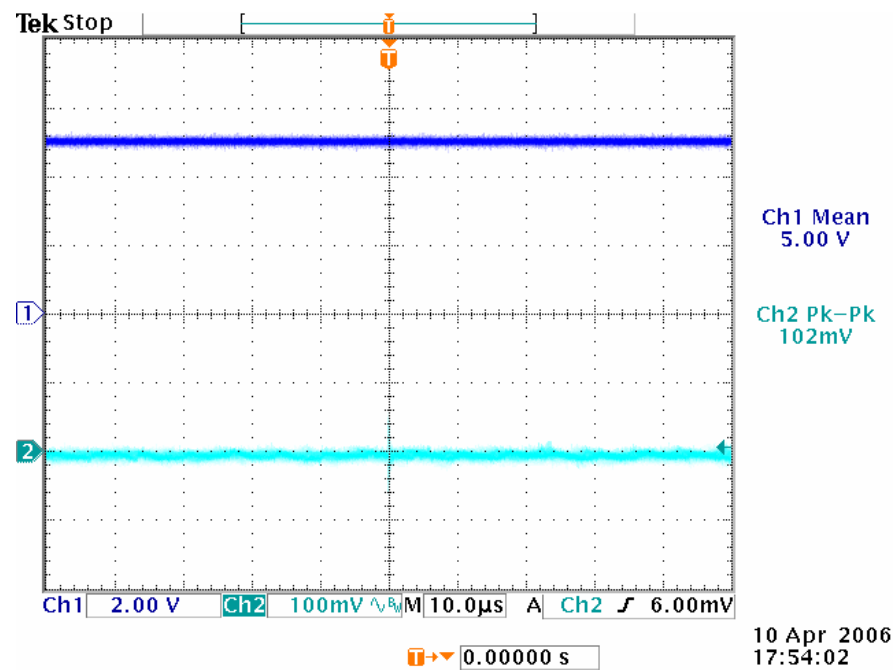
(1) 12V (DV120B, U6-1)



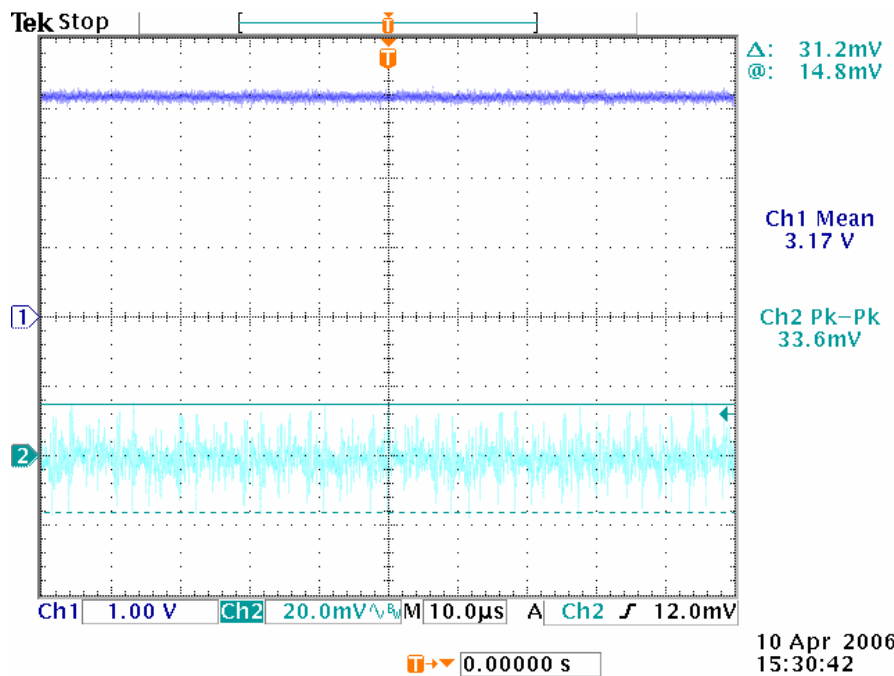
(2) 9V (AV\_V90, U6-3)



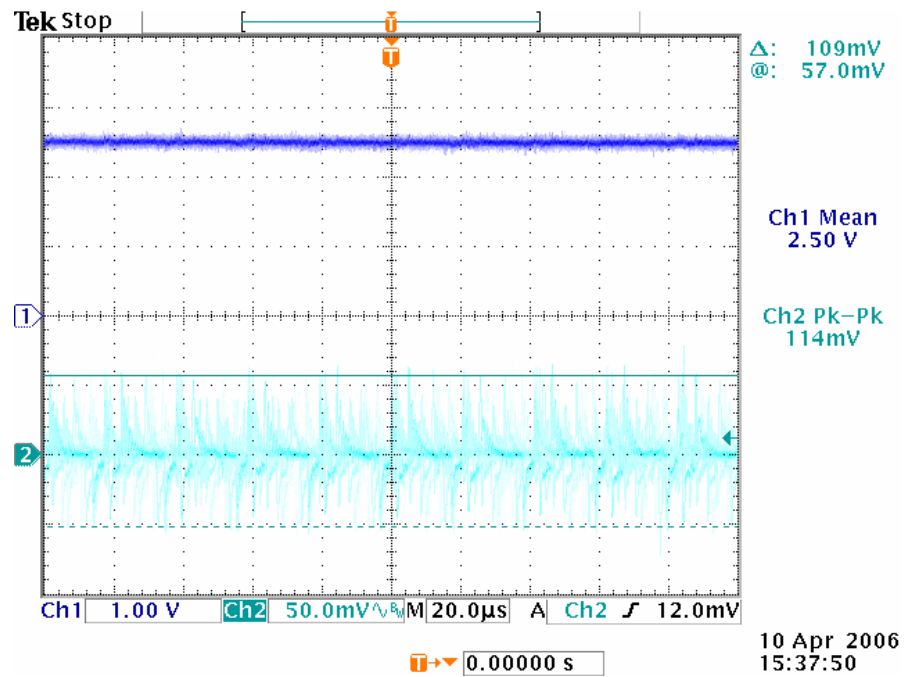
(3) 5V (DV50A, CB15)



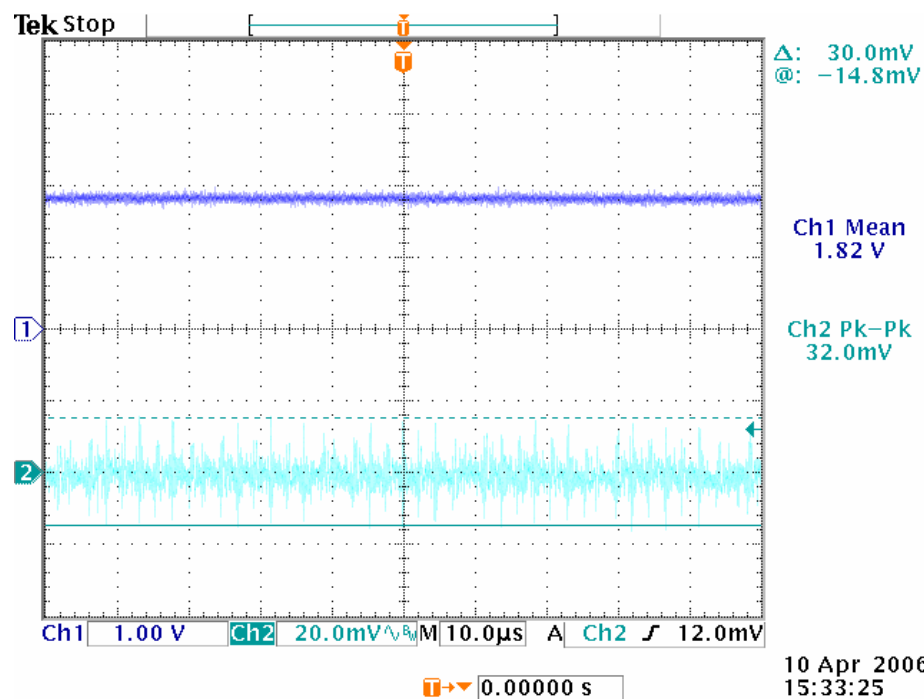
(4) 3.3V (DV33A, U5-3)



(5) 2.5V (DV25, CE42)

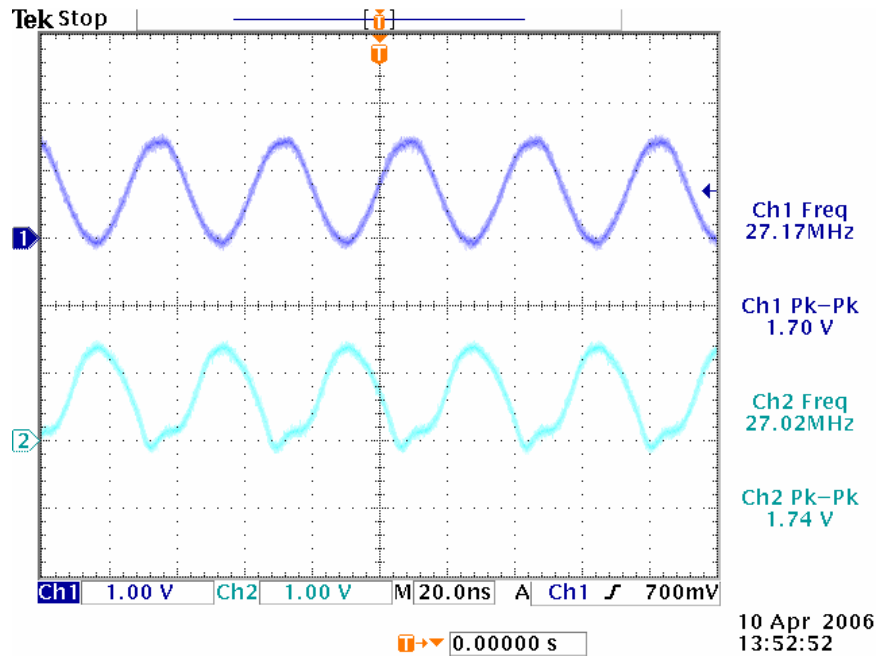


(6) 1.8V (DV18A, U5-2)

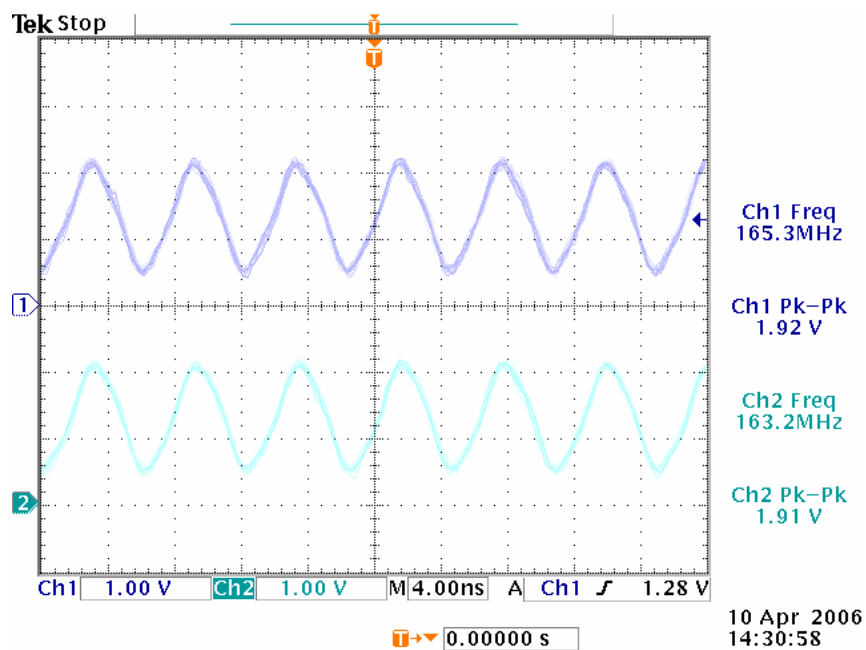


## 2. Clock Timing

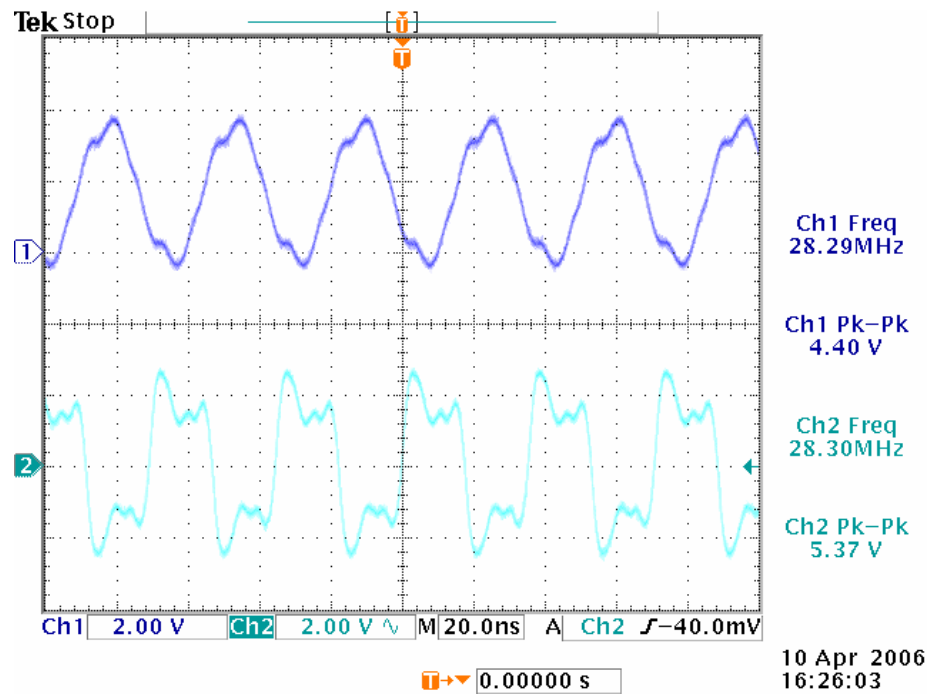
(1) MT8205 Clock (Ch1 U9-A15, XTALI / Ch2 U9-B15, XTALO)



(2) Memory Clock (Ch1 U11-45, D\_CLK / Ch2 U12-45, D\_CLK)



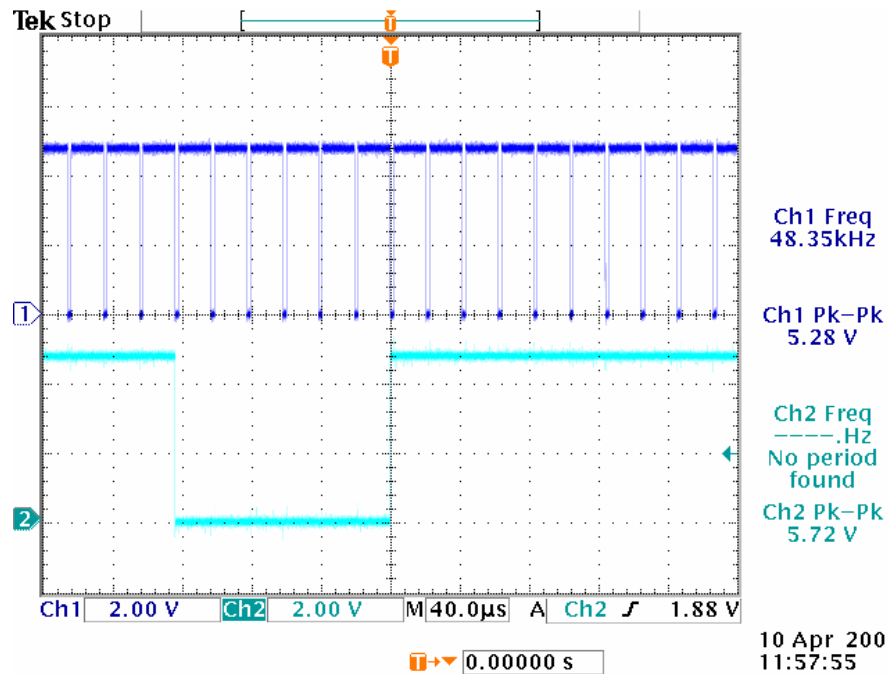
(3) Sil 9011 Clock (Ch1 U16-85, XTLI / Ch2 U16-84, XTLO)



### 3. H-sync & V-sync Timing

(1) PC Mode (1024 x 768 60Hz)

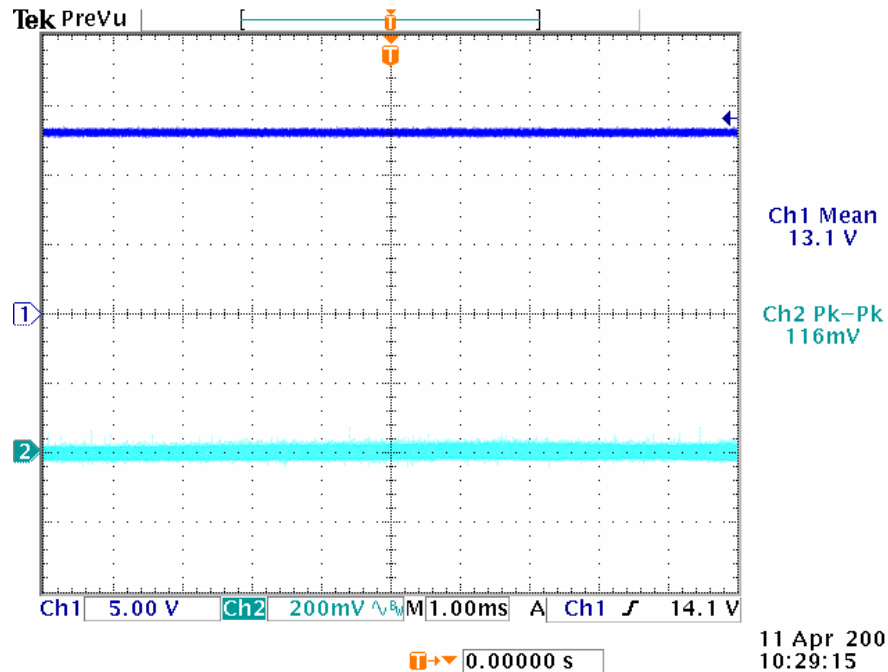
Ch1 H-sync (FB46) / Ch2 V-sync (FB45)



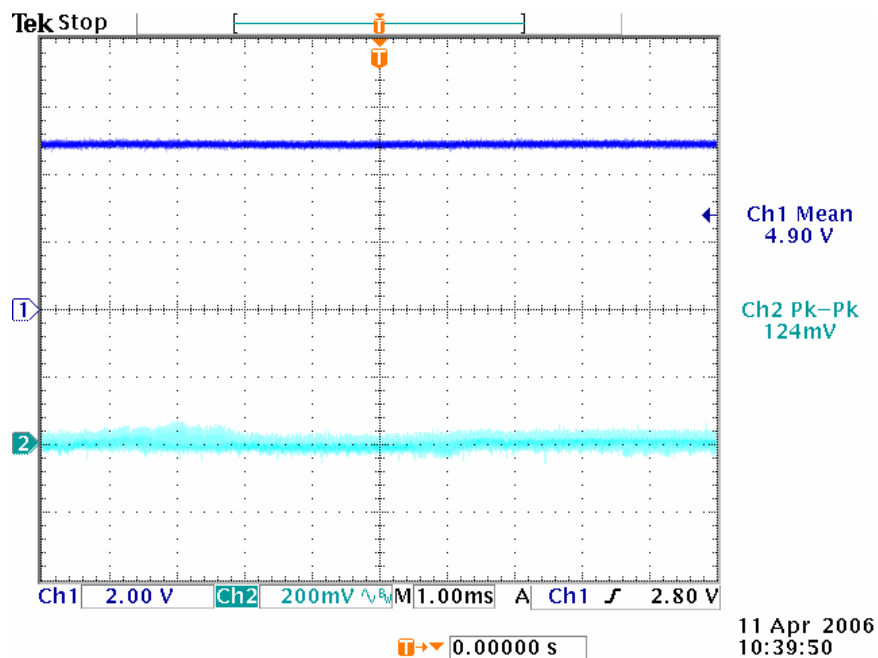
## ATSC Board

### 1. Voltage Measurement

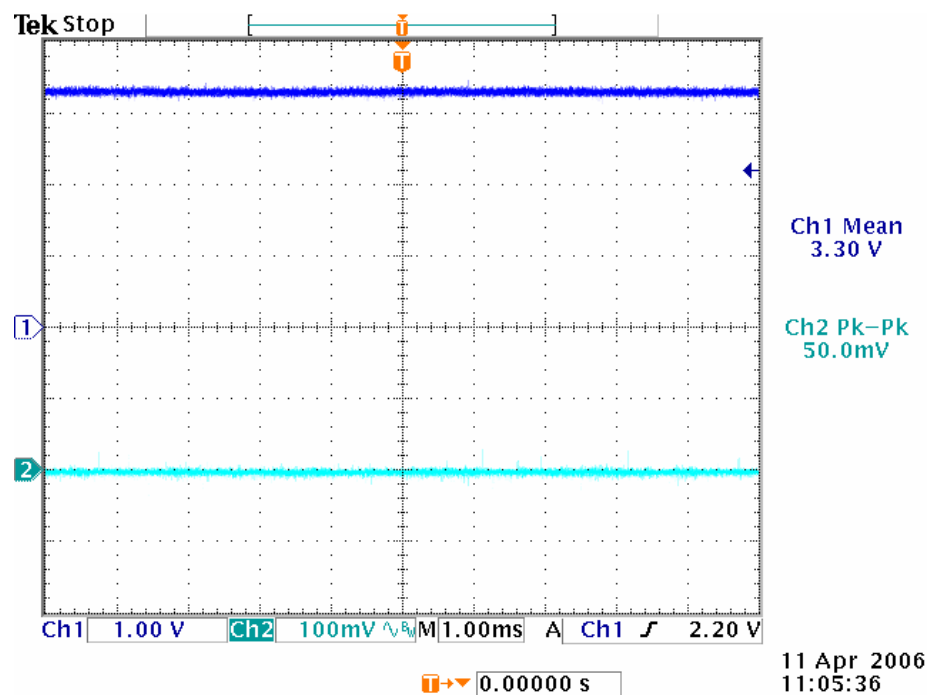
#### (1) 12V (+12V, C4)



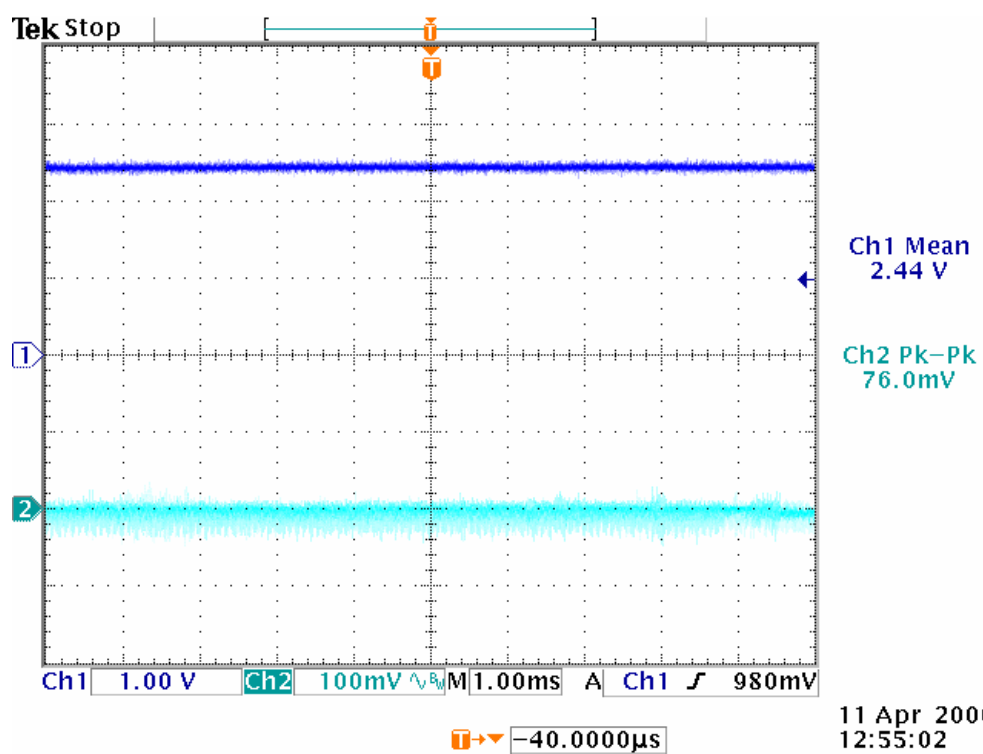
#### (2) 5V (+5V, C239)



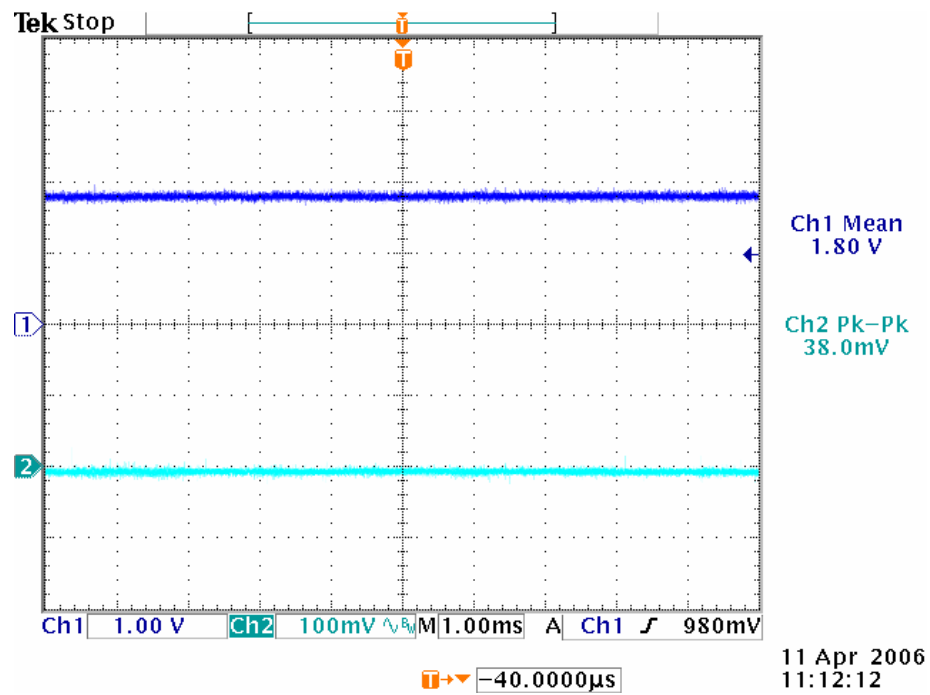
(3) 3.3V (DV33, C11)



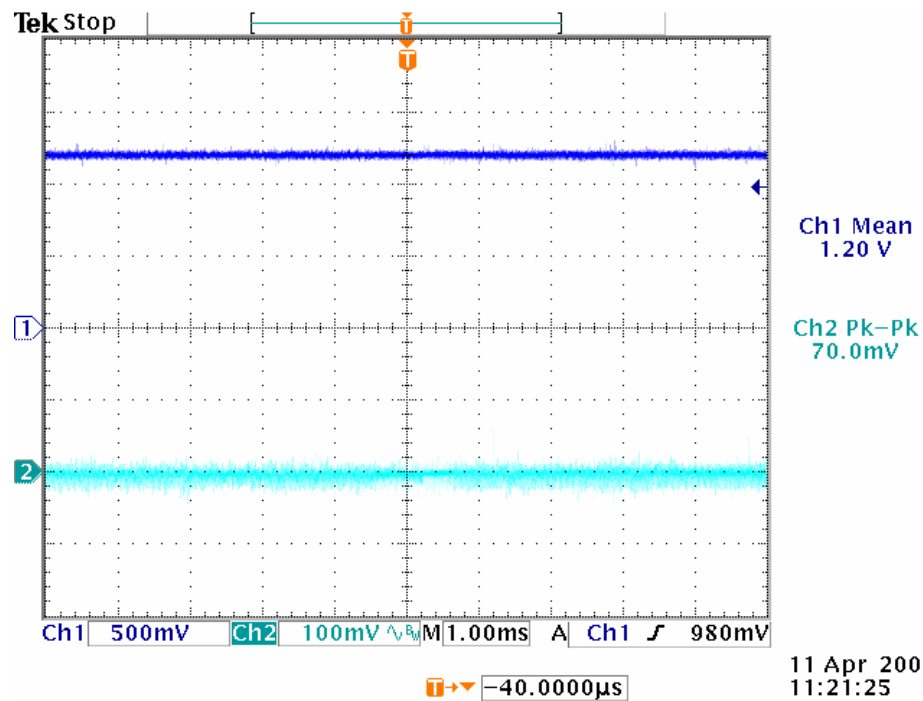
(4) 2.5V (DV25, C185)



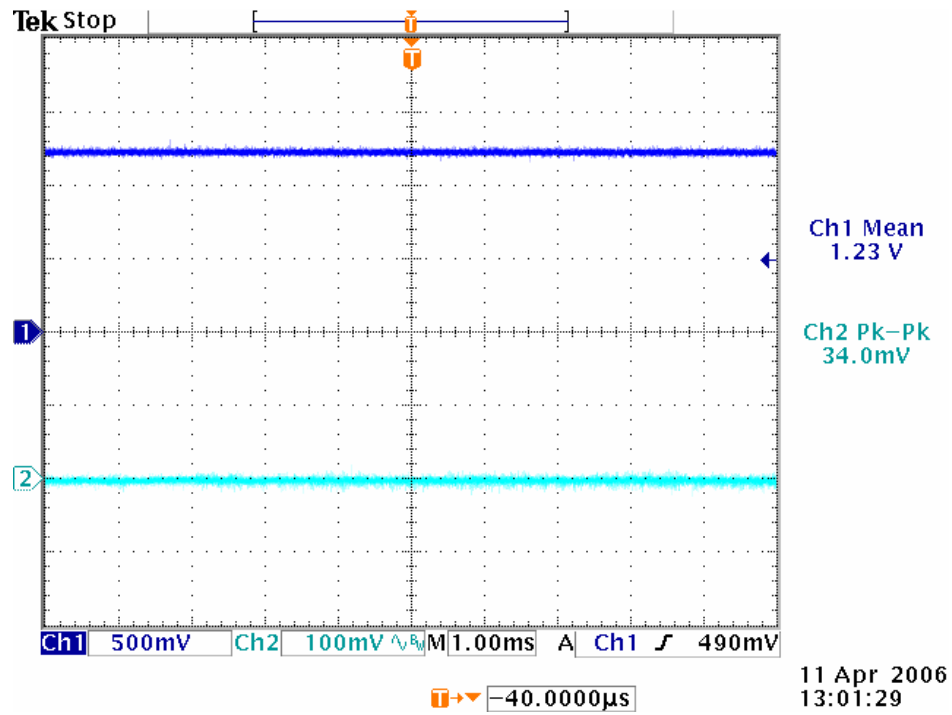
(5) 1.8V (DV18, C64)



(6) 1.25V (+1V25\_DDR, C148)

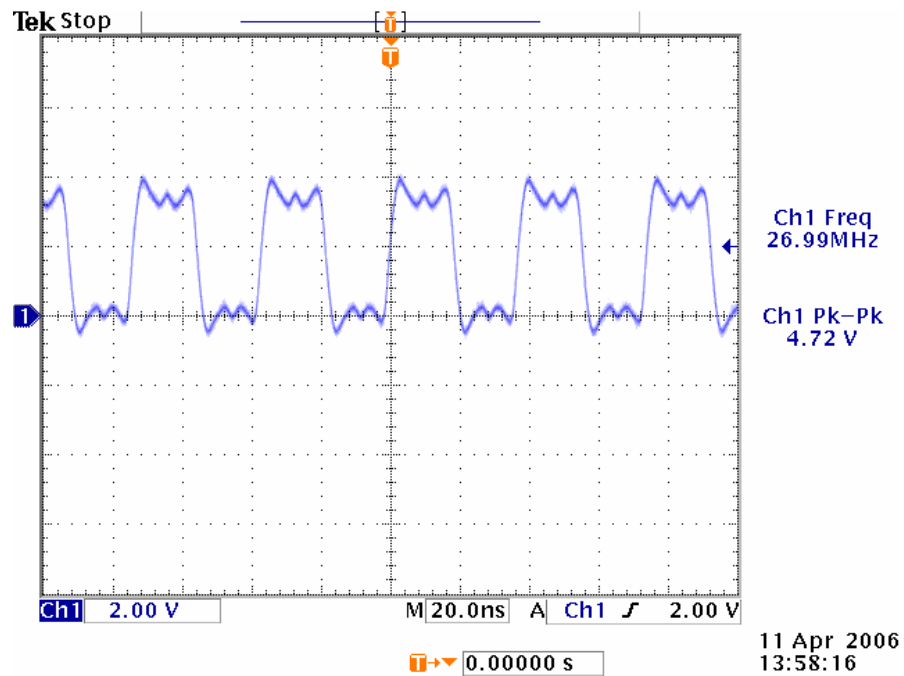


(7) 1.2V (DV12, C26)

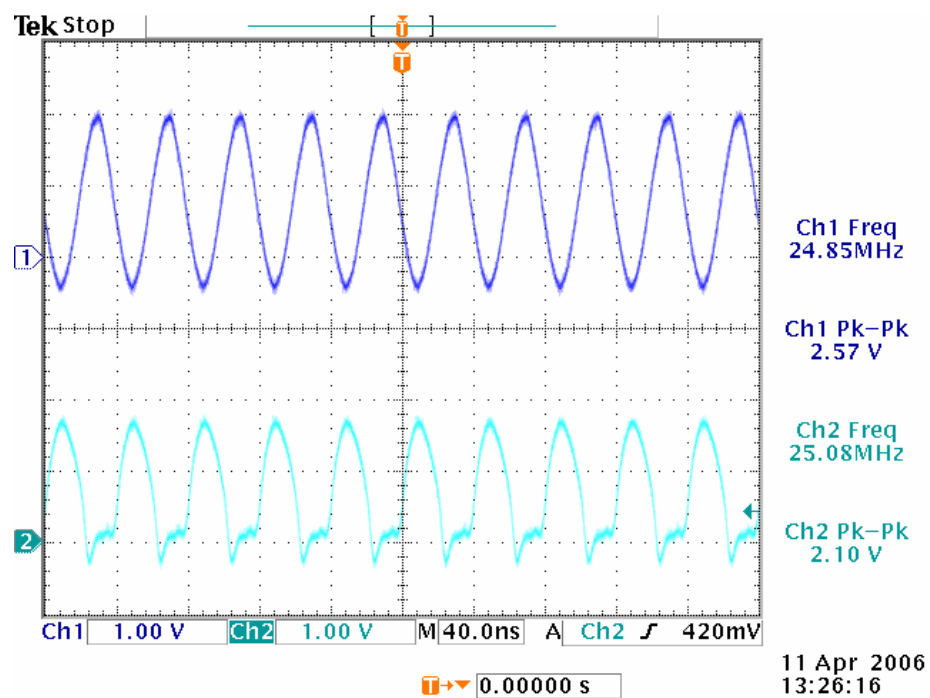


## 2. Clock Timing

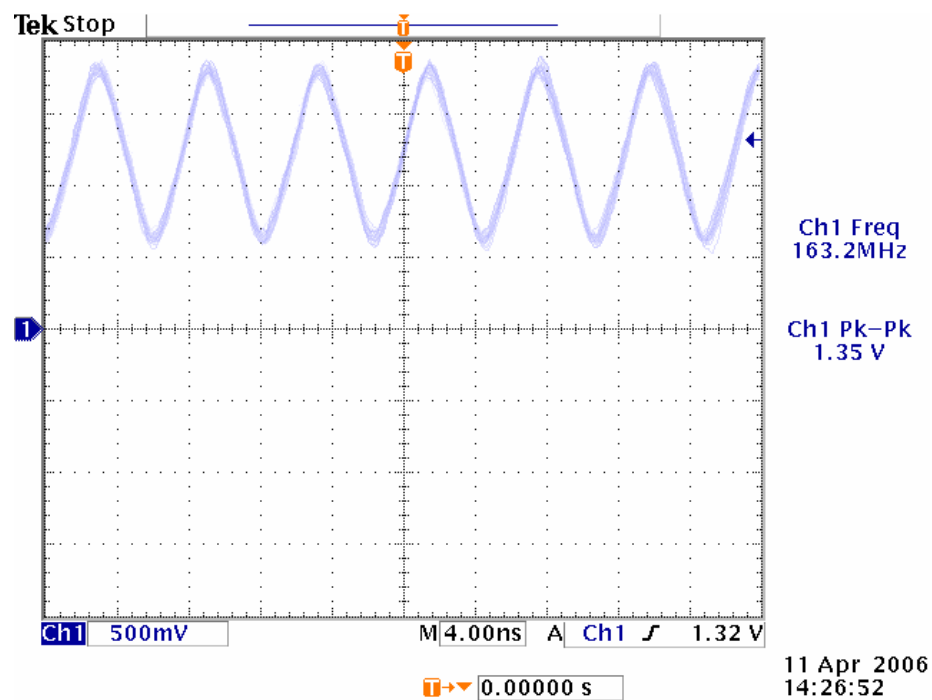
### (1) MT5351 Clock Timing (U10 B2-OXTALI)



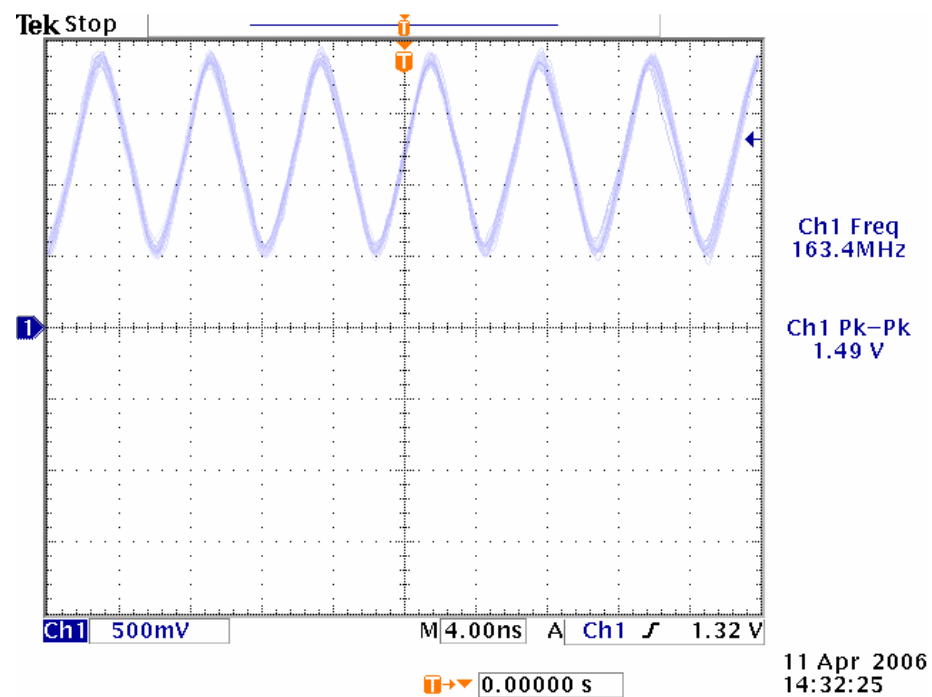
### (2) MT5111 Clock Timing (U9 97-XTAL1 / 96-XTAL2) Ch1 – XTAL1 / Ch2 – XTAL2



### (3) Memory Clock Timing (U13-45, MEM\_CLKA)

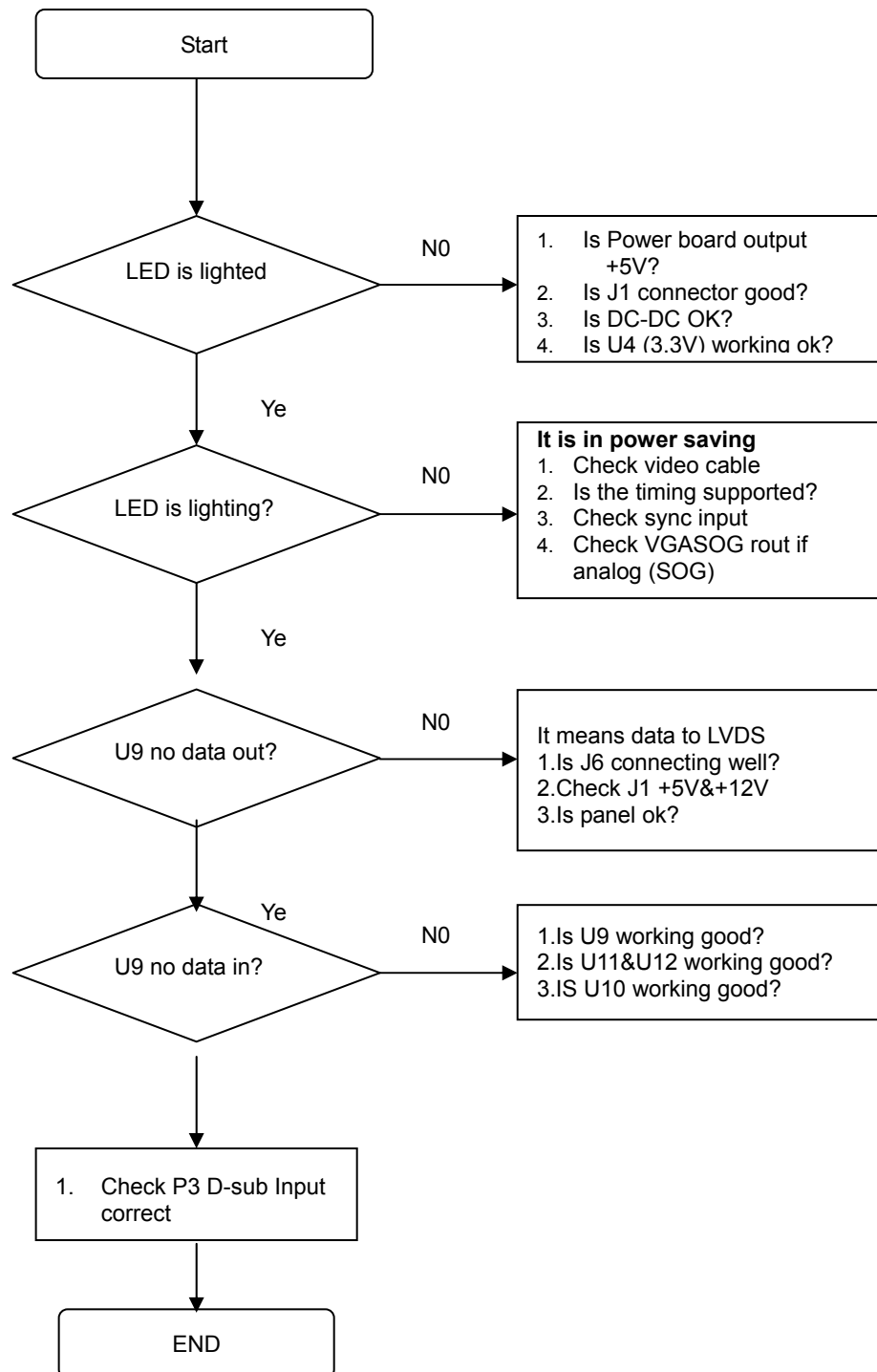


### (4) Memory Clock Timing (U12-45, MEM\_CLKA)



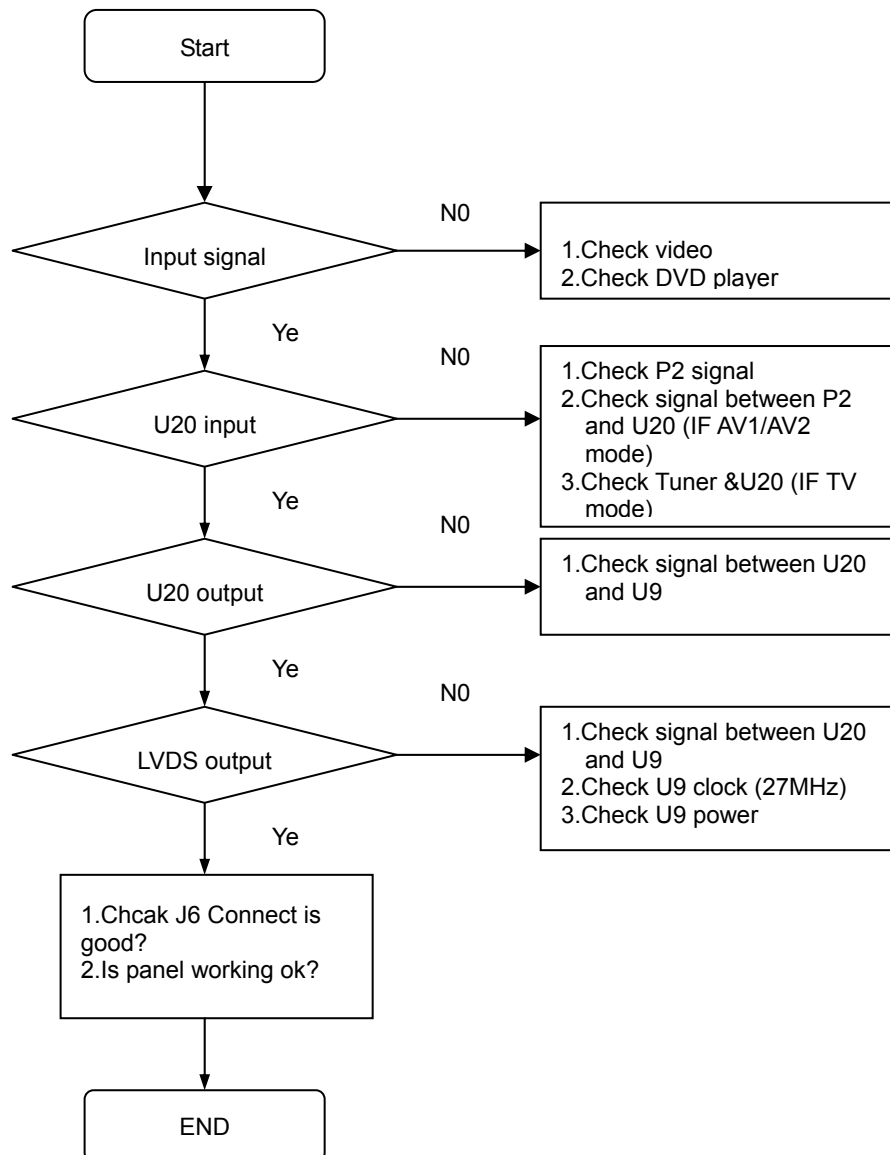
# Chapter 10    Trouble shooting

## MONITOR DISPLAY NOTHING (PC MODE)



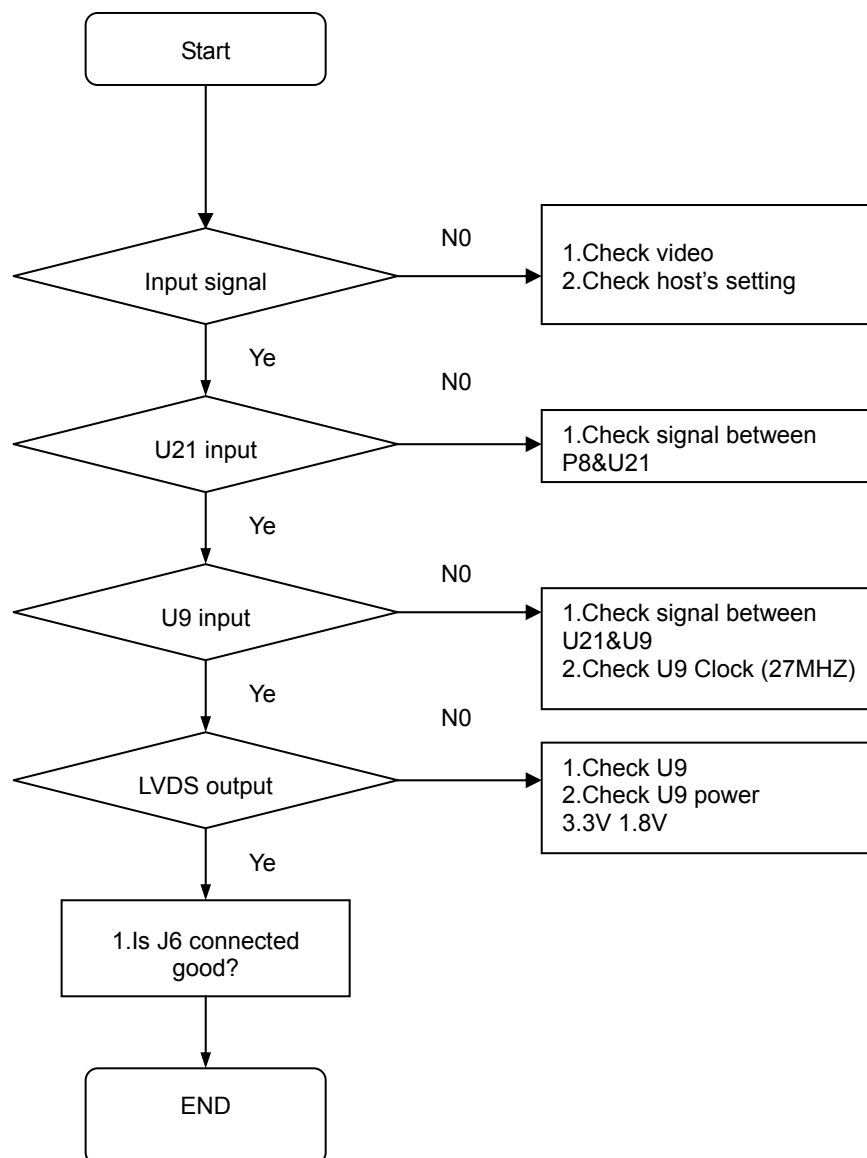
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(TV, COMPOSITE VIDEO1, 2, 3, S-VIDEO) IS NOT DISPLAY CORRECTLY



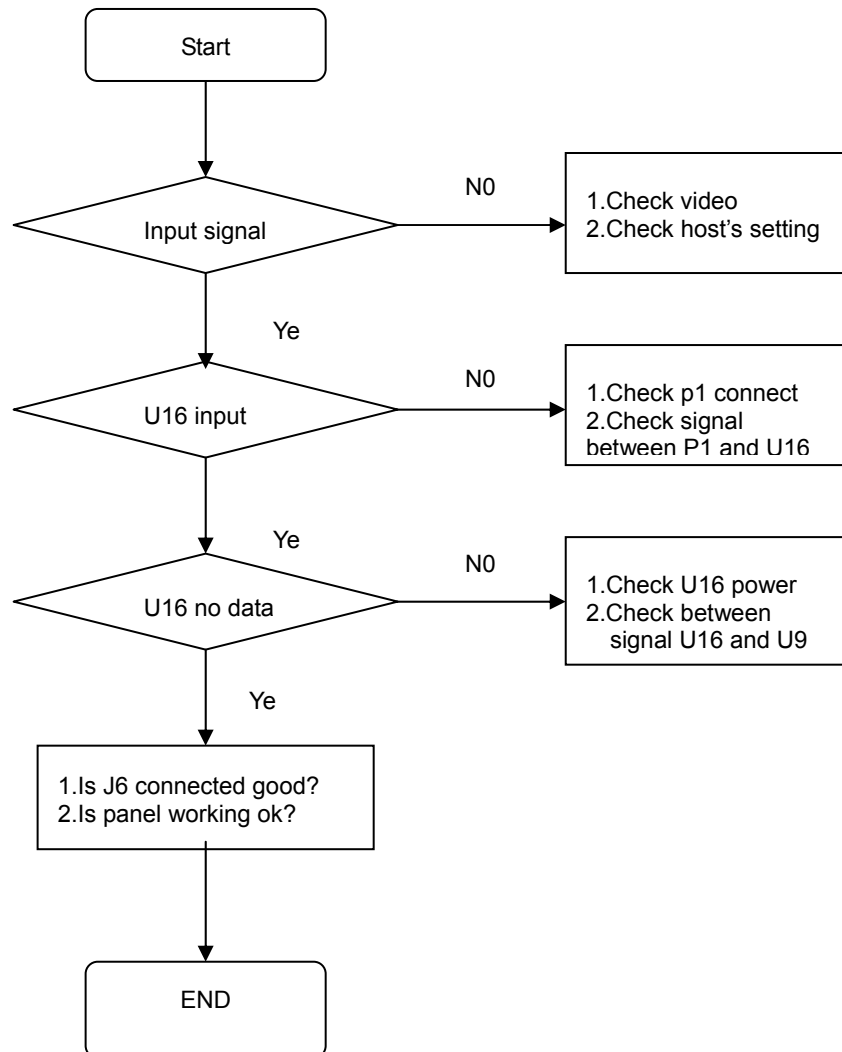
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(COMPONENT1, 2) IS NOT DISPLAY CORRECTLY

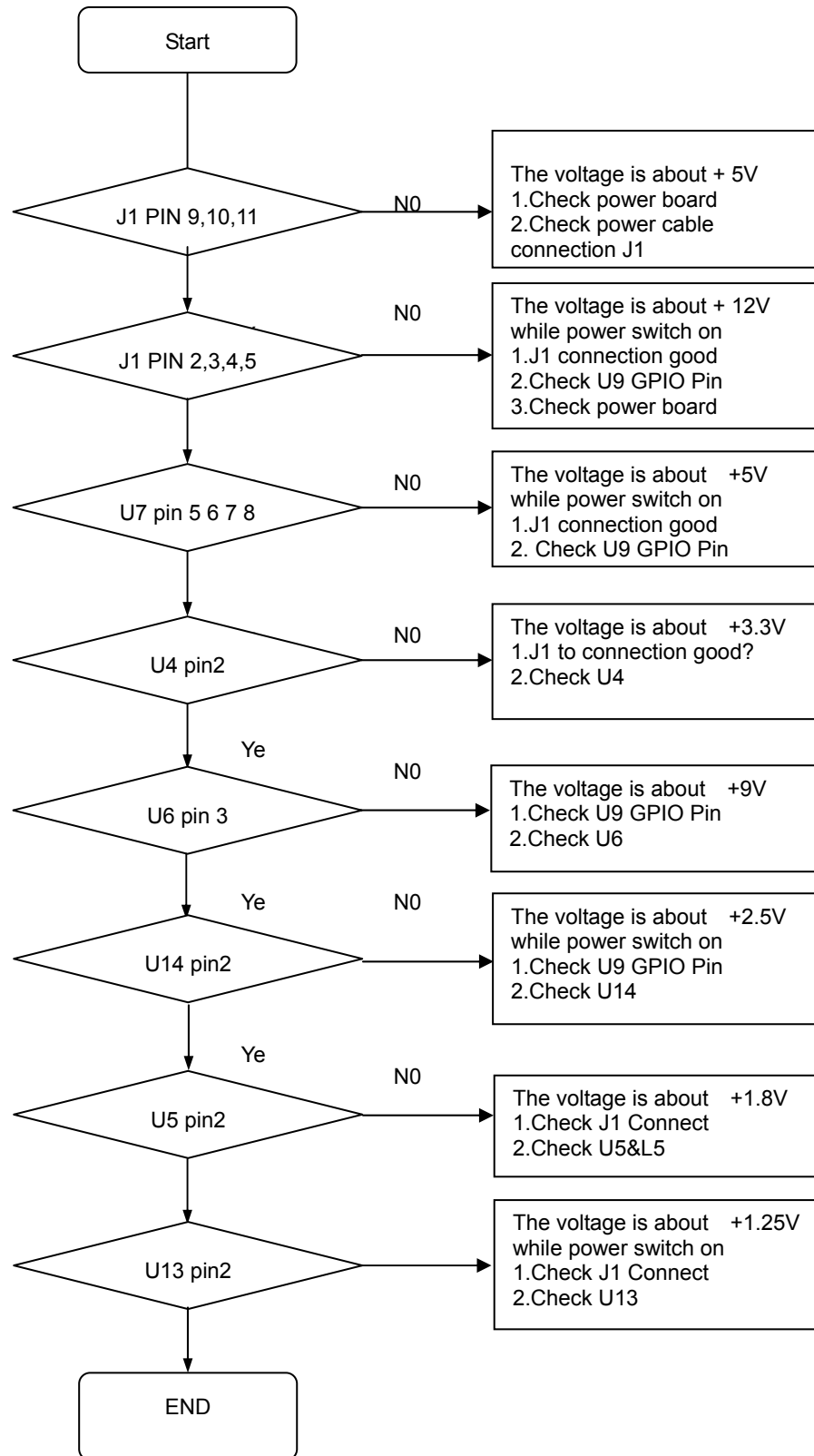


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(HDMI) IS NOT DISPLAY CORRECTLY

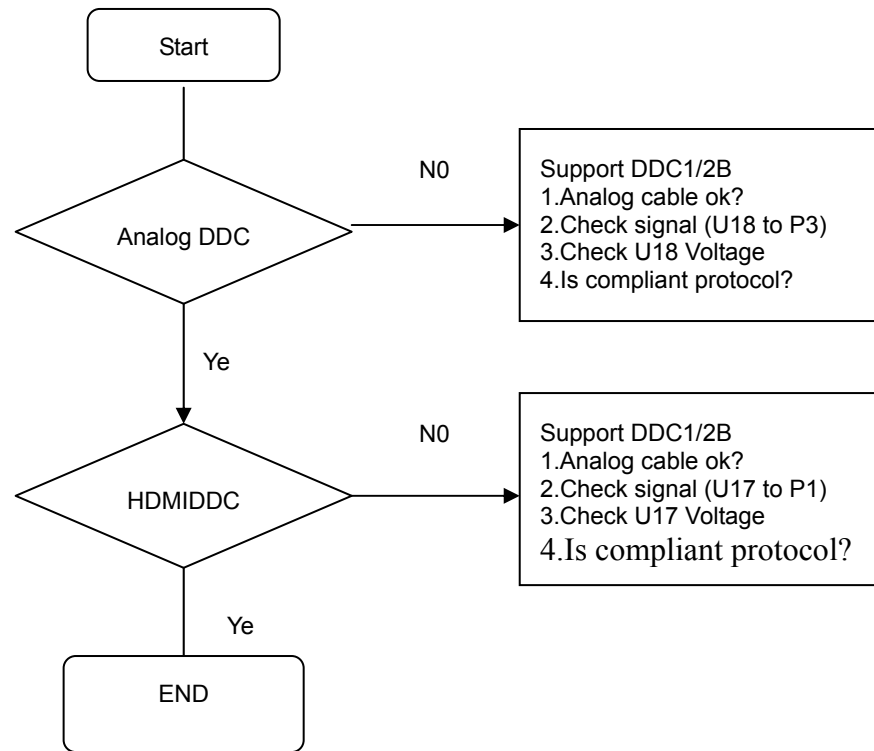


## TROUBLE OF DC-DC CONVERTER



---

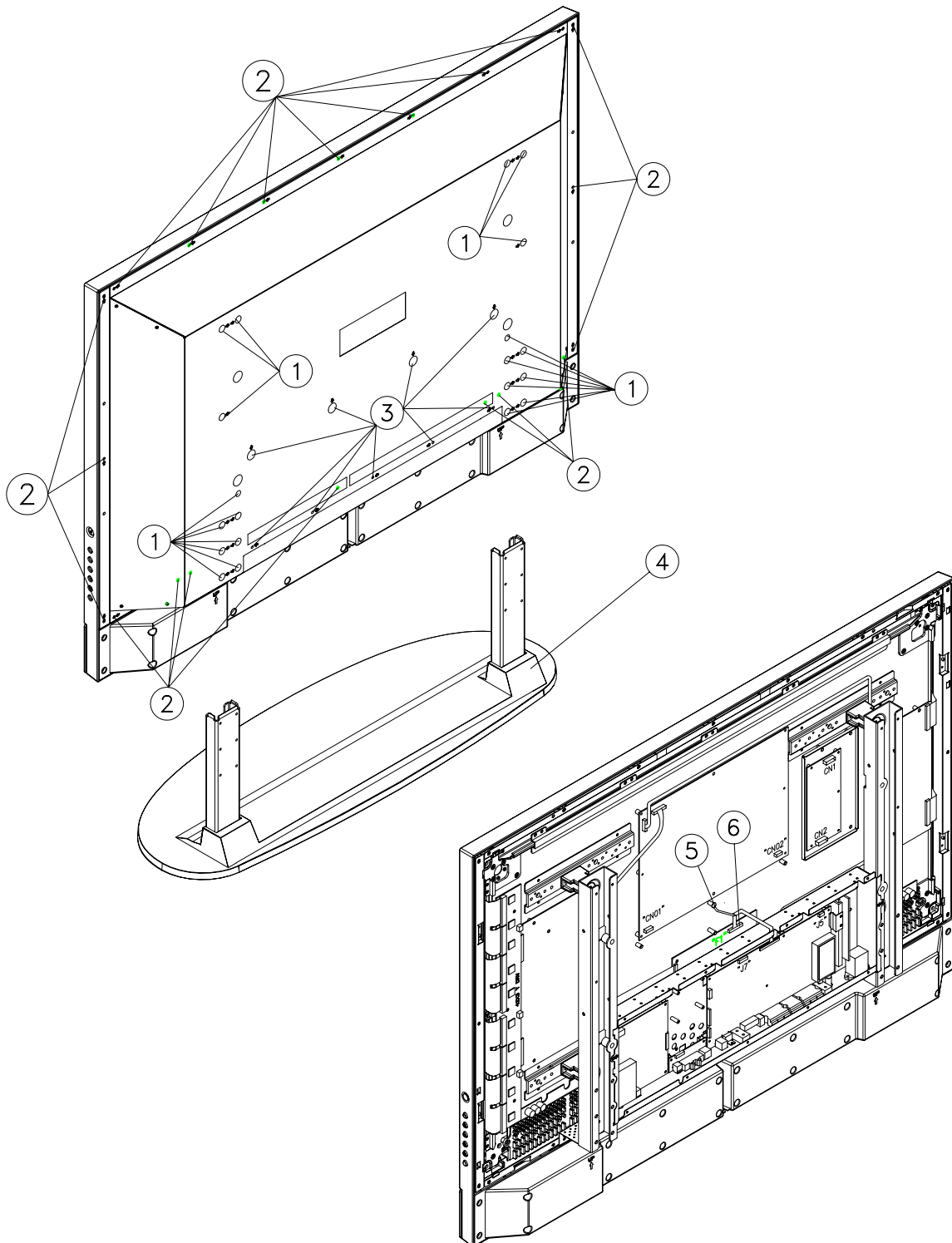
## TROUBLE OF DDC READING



## 1. REAR COVER ASS'Y REMOVAL

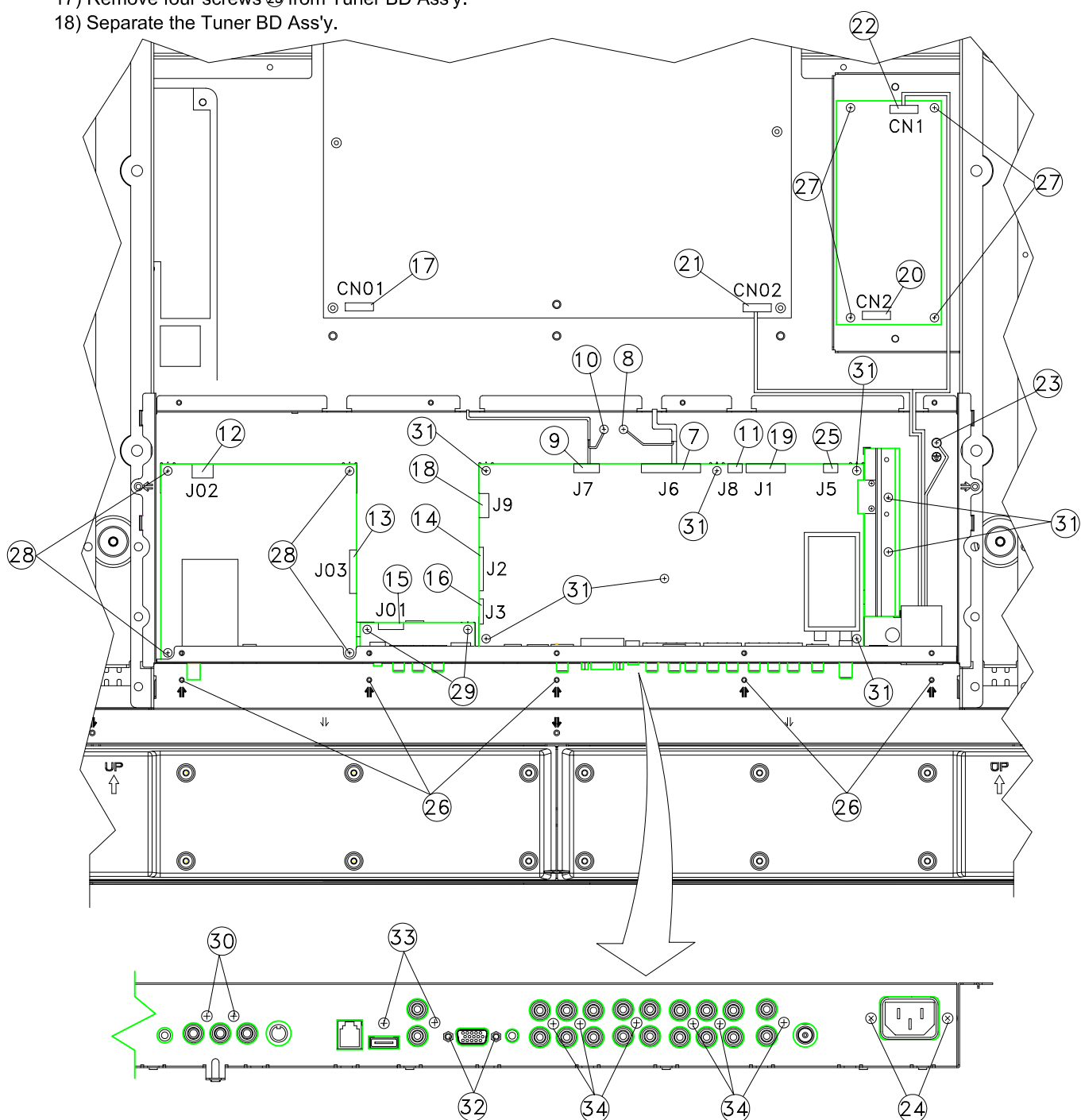
*Note: Spread a mat underneath to avoid damaging the Plasma surface.*

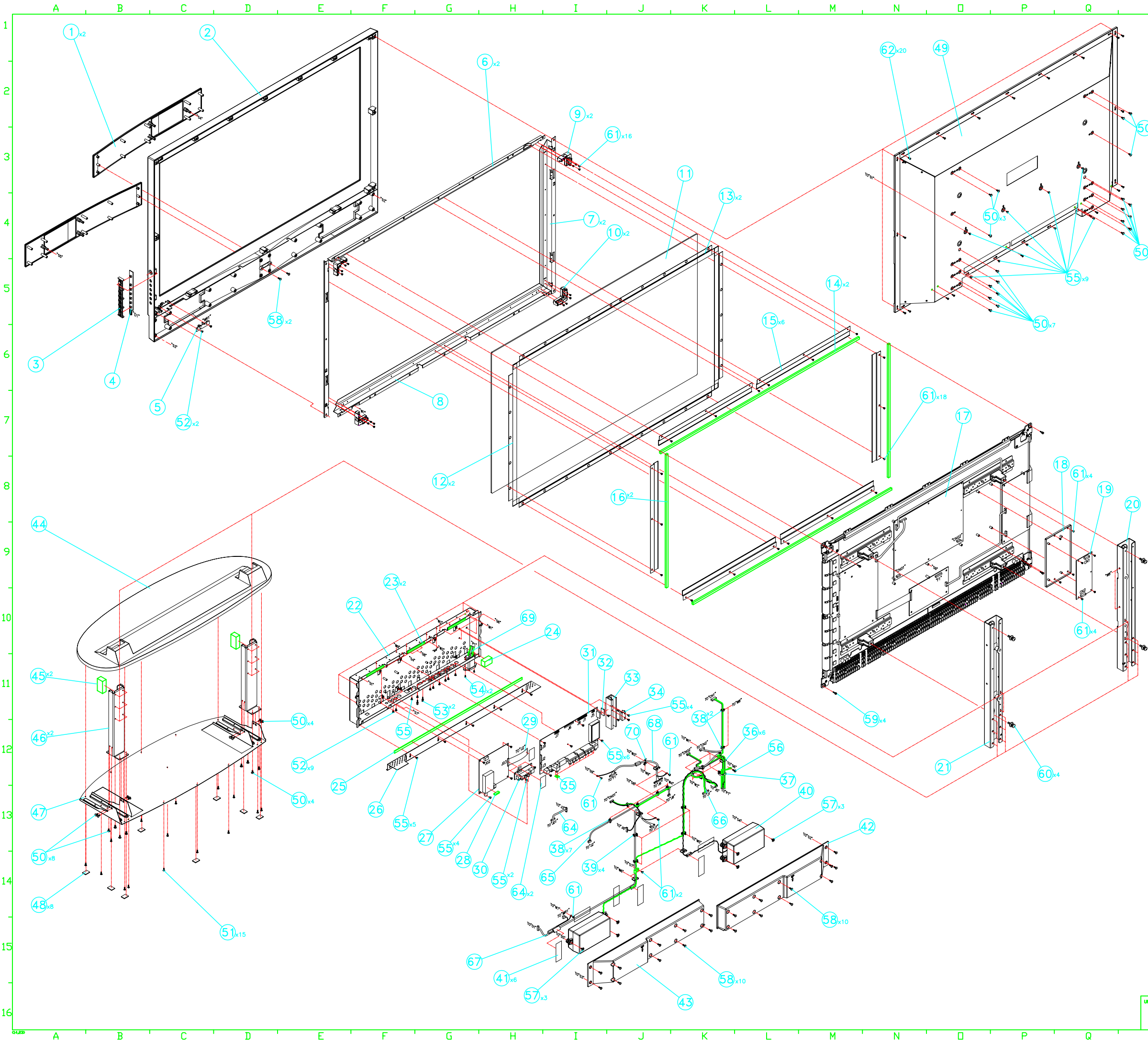
- 1) Remove twenty screws ① from rear cover.
- 2) Separate the Bass Ass'y ④.
- 3) Remove twenty screws ② and nine screws ③ from rear cover.
- 4) Separate the rear cover.
- 5) Remove the connector ⑥ (F1) of the LVDS cable.
- 6) Remove one screw ⑤.



## 2. MAIN BD ASS'Y REMOVAL


- 1) Remove the connector ⑦ (J6) of the LVDS cable.
- 2) Remove two screws ⑧ ⑩ from PCB support.
- 3) Remove the connector ⑨ (J7) of the keypad +IR cable.
- 4) Remove the connector ⑪ (J8) ⑫ (J02) of the Tuner cable.
- 5) Remove the connector ⑬ (J03) ⑭ (J2) of the FFC cable.
- 6) Remove the connector ⑮ (J01) ⑯ (J3) of the connector cable.
- 7) Remove the connector ⑰ (CN01) ⑱ (J9) ⑲ (J1) ⑳ (CN2) of the Power BD cable1.
- 8) Remove the connector ㉑ (CN02) ㉒ (CN1) of the Power BD cable2.
- 9) Remove one screw ㉓.
- 10) Remove two screws ㉔ from power cable Ass'y.
- 12) Separate the power cable Ass'y.
- 13) Remove the connector ㉕ (J5) of the speaker cable.
- 14) Remove five screws ㉖ from IO BKT.
- 15) Remove four screws ㉗ from power BD 2 Ass'y.
- 16) Separate the power BD2 Ass'y
- 17) Remove four screws ㉘ from Tuner BD Ass'y.
- 18) Separate the Tuner BD Ass'y.
- 19) Separate the Tuner BD Ass'y.
- 20) Remove two screws ㉙ and two screws ㉚.
- 21) Separate the connector BD Ass'y.
- 22) Remove eight screws ㉛ from Main BD Ass'y.
- 23) Remove two screws ㉜ and eight screws ㉝ from PCB support.
- 24) Separate the Main BD Ass'y.





ITEM	PART NO.	DESCRIPTION	QTY
1	1701-1926-1010	SPEAKER NET(PD-42L)	2
2	1801-0120-8010	FRONT BEZEL(PD-42L)ASS'Y	1
3	1701-0416-0010	BUTTON(PD-50LM)(PC,BLACK)	1
4	3842-0042-0156	DISPLAY BD ASS'Y D4237	1
5	3842-0072-0189	PDP IR BD ASS'Y(PD-42L)	1
6	1701-0416-0010	FILTER BRACKET HOR TOP(PD-42L)(SPGC T=0.8mm)	1
7	1712-0200-0160	FILTER BRACKET-VER(PD-42L)(SPGC T=0.8)	2
8	1712-0200-0150	FILTER BRACKET HOR BOTTOM(PD-42L)(SPGC T=0.8mm)	1
9	1701-0800-1580	FILTER BRACKET SUPPORT-2(PD-42L)	2
10	1701-0800-1570	FILTER BRACKET SUPPORT-1(PD-42L)	2
11	1701-0900-1760	PDP Filter 42" FG422NAA-05(FPR LG_PDP42X3)	1
12	1947-1800-0960	CONDUCTIVE FABRIC TAPE L584*W39	2
13	1947-1800-0970	CONDUCTIVE FABRIC TAPE L982*W39	2
14	1947-1500-2410	PANEL CUSHION(LENGTH=950mm)(PD-42L)	2
15	1712-0500-1590	FILTER CLIP(SPTE=0.3mm)(PD-42L)	6
16	1947-1500-2420	PANEL CUSHION(LENGTH=550mm)(PD-42L)	2
17	0213-0420-1161	PDP MODULE 42"PDP42X3(LG.PHILIPS)	1
18	1712-0200-0440	POWER BRACKET(PD-42L)	1
19	0500-0502-0160	POWER BD ASS'Y LF	1
20	1712-0200-0270	MAIN FRAME-R(PD-42L)(SPGC T=2.0mm)	1
21	1712-0200-0280	MAIN FRAME-L(PD-42L)(SPGC T=2.0mm)	1
22	1712-0200-0200	PCB SUPPORT(SPGC T=0.8mm)	1
23	1947-1800-0390	GASKET BLOCK (6W*1H*80Lmm)	3
24	1947-1800-1000	GASKET BLOCK(35.0L*21.0W*17.0H)	1
25	1947-1800-0990	IGASKET BLOCK L576*W8*H2mm(PD-42L)	1
26	1712-0200-0190	IO BRACKET(PD-42L)(SPGC T=0.8mm)	1
27	3842-0022-0190	PDP TUNER BD ASS'Y(PD-42L)	1
28	1947-1800-0370	GASKET BLOCK(5.5H*10.0W*30.0Lmm)	1
29	0460-2850-0100	FFC 50P(0.5mm) 105mm	1
30	3842-0072-0146	CONNECTOR BD ASS'Y(PD-42L)	1
31	3842-0122-0150	PDP MAIN BD ASS'Y(PD-42L)	1
32	1947-1900-0030	HEATPATH (25X14mm)	1
33	1712-0400-0720	HEAK SINK(PD-42L)	1
34	1712-0100-4590	HEAT SINK FIX MTEAL(TM-30A)	1
35	1947-1800-0290	GASKET BLOCK(12L*10W*15.Hmm)Hole ø6	1
36	1701-1500-1080	WIRE SADDLE DS-12(NYLON)	6
37	1701-1500-0690	WIRE SADDLE(CH-14)	1
38	1701-1500-0450	WIRE SADDLE(CH-01B)	7
39	1701-1500-0220	WIRE SADDLE(CH-02)	4
40	0355-1006-0350	SPEAKER ASS'Y 60HN 10W BOX+WIER670/890mm	6
41	1947-1200-0310	ACETATE CLOTH TAPE(27*75mm)	1
42	1701-1926-2010	SP REAR COVER-R (PD-42L)	1
43	1701-1926-3010	SP REAR COVER-L (PD-42L)	1
44	1701-0520-2010	BASE COVER (PD-42L)(HIPS,877C)	1
45	1947-1800-0980	GASKET BLOCK L50*W17*H25	2
46	1712-0100-8980	BASE FRAME (PD-42L)(SPGC T=2.5mm)	2
47	1712-0100-8990	BASE-PLATE(PD-42L)(SECC T=1.2mm)	1
48	1701-1000-0520	FOOT(PORON)(20mm*15mm*2.0mm)	8
49	1712-0100-8970	REAR COVER(PD-42L)(SPGC T=0.8,BLACK)	1
50	1720-0004-0850	MAC.SCREW-MB M4.0*8.0L,BLK-NI	-
51	1721-3003-0920	TAP.SCREW-MF M3.0*9.0L,NI	15
52	1721-0003-0650	TAP.SCREW-TB#3.0*6.0L,BLK-NI	9
53	1720-7344-0820	MAC.SCREW-MHSW #4-40*8.0L,NI	2
54	1723-0047-1050	TAP.SCREW-TB#4.7*10.0L,BLK-NI	2
55	1720-0003-0650	MAC. SCREW-MB M3.0*6.0L,BLK-NI	-
56	1720-1204-0820	MAC.SCREW-MPGM M4.0*8.0L,NI	1
57	1721-4103-0820	TAP.SCREW-TRF#3.0*8.0L,NI	6
58	1721-0004-1250	TAP.SCREW-TP#4.0*12.0L,BLK-NI	22
59	1721-2103-1050	TAP.SCREW-TRFW#3.0*10.0L,BLK-NI	4
60	1720-2505-1020	MAC.SCREW-MR M5.0*10.0L,NI	-
61	1720-2003-0620	MAC.SCREW-MR M3.0*6.0L,NI	4
62	1721-0003-1050	TAP.SCREW-TB#3.0*10.0L,BLK-NI	20
63	1947-1200-0400	ACETATE CLOTH (20*45mm)	2
64	0460-1016-0030	WH PHDR16VS-PHDR16VS 1061#26 100mm	1
65	0460-1105-0090	WH XH5P-PH5P 1007#24 400mm	1
66	0460-1013-0100	WH PH13P-A2543H10P+E17P 1007#24 280/380mm CORE	1
67	0460-1012-0191	WH PH12P-ZH9P+PH4P 20276 927/972mmCORE*2	1
68	0460-3430-0690	WH P240430/FI-W31S 300mm	1
69	0460-1207-0010	WH VHR6P+178125-2 1617#22 400/430mm	1
70	1701-1500-1350	WIRE CLIP(TDY8-1A)	1

UNLESS OTHERWISE NOTED  
JX = #0.10  
X = #0.2  
ANG = 1/2"

VIZIO P42HDTV10A		2842-8500-3053	
DESCRIPTION		PART NO.	
AMTRAN TECHNOLOGY Co., LTD. DSN: JESSIE Yu 03/27/06 CHK:	THIRD ANGLE PROJECTION 	MODEL No.	VIZIO P42HDTV10A
	MATERIAL: 000000	DWG. NAME:	42" CASE ASS'Y
	QTY: 1 SIZE: A1	DWG. No. VIZIO-P42HDTV10A-01	
	SCALE: Full UNIT: MM	REV. 0	SHEET 1 of 1